2006

A 2.4GHz fast-switching integer-N frequency synthesizer

Sreenath Thoka
Iowa State University

A 2.4GHz fast-switching integer-N frequency synthesizer

by

Sreenath Thoka

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Randall L. Geiger, Major Professor
Degang J. Chen
Douglas W. Jacobson

Iowa State University

Ames, Iowa

2006

UMI Number: 1439926

ProQuest Information and Learning Company
300 North Zeeb Road
P.O. Box 1346
Ann Arbor, MI 48106-1346

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The adaptive bandwidth technique is commonly used to implement fast switching in low-spurious frequency synthesizers. In this technique the high loop bandwidth used during the switching mode has to be restored once switching is complete. The process of restoring the bandwidth adds to the total switching time because of the glitches on the VCO control voltage arising from the perturbation caused in the loop. Often in applications demanding ultra fast switching times and tight error tolerances, the additional settling time due to these secondary glitches can be a significant fraction of the total switching time. In this thesis, a more efficient multi-step bandwidth-switching scheme is proposed that can significantly reduce the total switching time by minimizing the effect of secondary glitches. After satisfactory behavioral simulations, a proof-of-concept test chip integrating a 2.4GHz Integer-N synthesizer is designed and fabricated in the TSMC 0.25μm mixed-signal CMOS process. Simulations using time contraction show that the synthesizer switches 14% faster in the four-step mode compared to the one-step mode for a frequency step of 20MHz and 0.1% error tolerance.

CHAPTER 1. INTRODUCTION

1.1. Motivation

Wireless communication standards such as Bluetooth and Wireless LAN (802.11) use frequency hopping for data security and better immunity to multi-path fading. Frequency hopping refers to the repeated switching of the carrier among different frequency channels during transmission. A Phase Locked Loop (PLL) based fully integrated frequency synthesizer that can generate multiple frequencies using a single reference frequency offers an efficient implementation for frequency hopping more so with the current advancements in CMOS process technology. Some frequency hopping systems use rapid switching of frequencies demanding a tight specification on the synthesizer switching time. A common approach to achieve rapid switching is to "ping-pong" two synthesizers resulting in nearly zero switching time since one synthesizer is already switched to the next frequency in the hopping sequence while the other is providing the carrier. This approach proves to be inefficient for present day battery-operated miniature wireless devices. A single frequency synthesizer that can meet the tight switching time specifications is highly desirable.

Implementing a fast-switching synthesizer involves design trade-offs, with the open loop bandwidth (or simply loop bandwidth) usually being the trade-off parameter. The loop bandwidth defined as the cross over frequency of the loop gain affects the switching time and spurious requirements in a conflicting manner. Also the loop bandwidth is theoretically a small fraction of the reference frequency, which in the case of Integer-N (output frequency is an integer multiple of reference frequency) synthesizers cannot exceed channel spacing thereby making the trade-off more severe. A commonly used solution to relax the trade-off is an adaptive bandwidth synthesizer in which initial lock to the new frequency is obtained in a high-bandwidth mode and the bandwidth is restored thereafter for better spurious performance. The total switching time of adaptive bandwidth synthesizers includes the initial

lock time and the additional time for restoring the bandwidth. Consider a synthesizer with a loop bandwidth of f_C that switches from frequency f_1 to f_2 in 200μs. Increasing the bandwidth to $4f_C$ results in a switching time of 50μs (switching time is inversely proportional to loop bandwidth as will be shown in the following Chapters). However the bandwidth has to be restored from $4f_C$ to f_C after frequency f_2 becomes valid. Thus the total switching time is 50μs + t_{HL} as shown in Figure 1-1, where t_{HL} is the additional time for restoring the bandwidth to its nominal value.

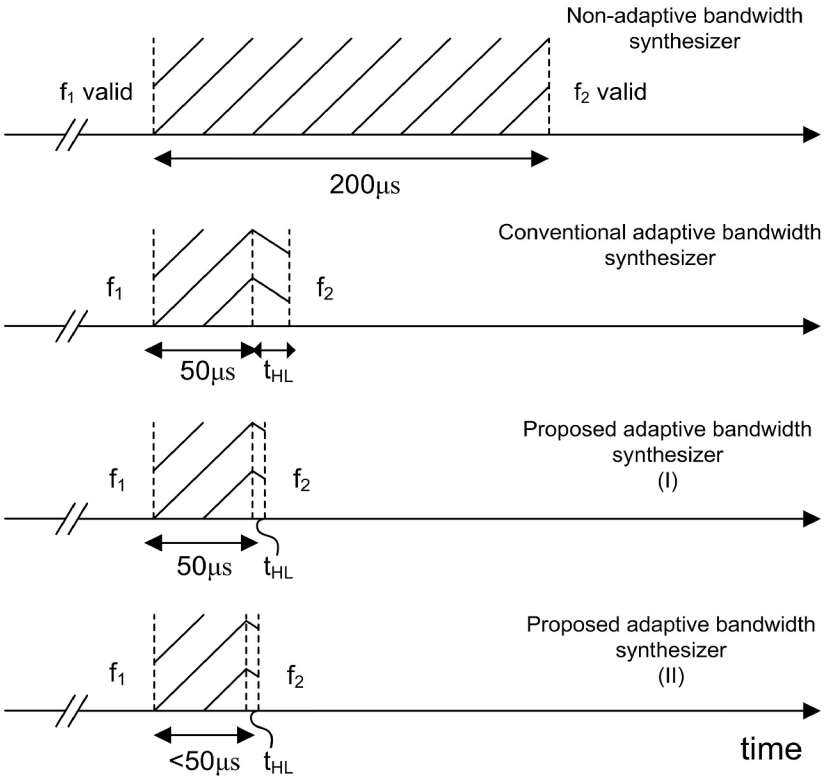

Figure 1-1 Objective of the Thesis

t_{HL} can be a significant fraction of the total switching time depending on the method of restoring bandwidth, the initial lock time and the frequency error that can be tolerated. To take complete advantage of the high bandwidth mode, t_{HL} must be an insignificant fraction of the total switching time. The key to reducing t_{HL} is to minimize the perturbation caused in the 'already-settled' loop when bandwidth is restored. The objective of this thesis is to adapt the

conventional adaptive bandwidth architecture such that t_{HL} can be significantly reduced, as shown for proposed architectures (I) and (II) in Figure 1-1, resulting in an optimal total switching time. With the proposed architecture (II), the initial lock and t_{HL} phases can be overlapped to further optimize the total switching time.

1.2. Thesis Organization

The following Chapter presents the theory of frequency synthesizers. Starting with the basic architecture, linear models are developed and relevant properties of the feedback loop are studied to lay the foundation for Chapter 3 where the main focus of this work is discussed. Specifically, in Chapter 3 performance parameters of a synthesizer causing a design trade-off, are considered and an existing solution for relaxing the trade-off and achieving fast switching is presented with an emphasis on its limitations. A new architecture is then proposed that has the potential to overcome the limitations of the existing architecture.

Chapters 4 and 5 discuss in detail the design of the synthesizer using the architecture proposed in Chapter 3. In Chapter 4, specific modifications and additions to the conventional architecture that result in the proposed architecture are mentioned. System-level parameters are specified and used to derive design parameters for the circuit implementation discussed in Chapter 5. Design of the basic building blocks, additional building blocks required by the proposed architecture and the supplementary blocks useful for debugging and interfacing with the real world, is presented in Chapter 5. Chapter 6 starts by considering practical issues in synthesizer simulation and then presents the results for transistor-level switching time simulations using a speed-up technique. The simulation results for the building blocks are also presented in this Chapter. Chapter 7 discusses experimental results. Some information about layout, fabrication process and packaging is provided before discussing measured results. Chapter 8 provides a conclusion for the thesis.

CHAPTER 2. FUNDAMENTALS OF FREQUENCY SYNTHESIZERS

2.1. Background

A frequency synthesizer is essentially a Phase-Locked Loop (PLL) in which feedback is used to lock the output frequency and phase to the frequency and phase of a stable reference. Using a programmable frequency divider in the feedback loop of a PLL leads to an efficient way of generating output frequencies that are an exact multiple of the reference frequency. Figure 2-1 shows the block diagram of the synthesizer. The phase frequency detector (PFD) generates an error signal that is a function of the phase difference between the reference (REF) and the feedback (OSC) signals. The charge pump (CP) converts the error signal into equivalent current pulses that are filtered by the loop filter (LPF) to produce the control voltage for the voltage-controlled oscillator (VCO). The VCO control voltage adjusts the output (OUT) frequency such that the frequencies of the reference and the feedback signals are equal.

$$f_R = \frac{f_O}{N} \tag{2-1}$$

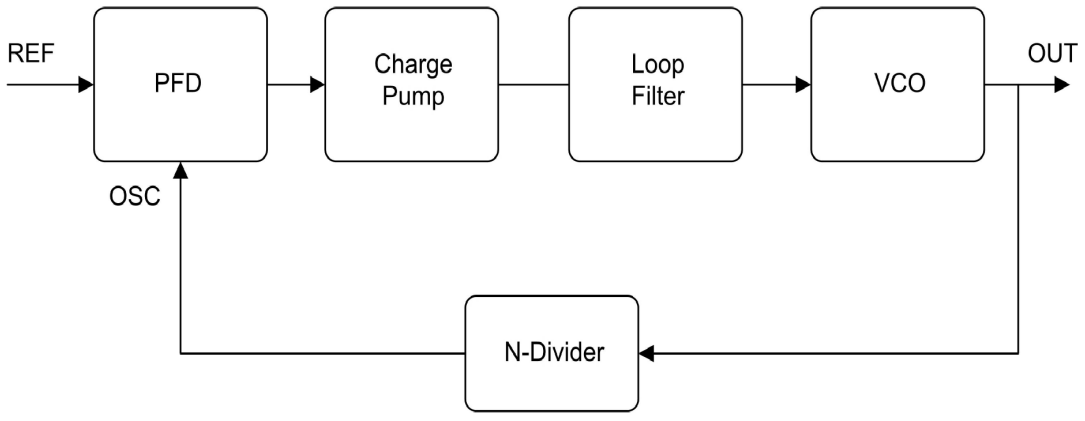

Figure 2-1 Block Diagram of Frequency Synthesizer

2.2. Linear Model of Synthesizer

A linear model of a synthesizer provides good insight for evaluating its transient behavior, noise performance and stability. The feedback signal in a synthesizer is the phase of the divided VCO output. For small phase errors in the vicinity of the locked state the synthesizer can be accurately described by a linear model in the S-domain.

Figure 2-2 shows the linear model of the synthesizer. The transfer functions for each of the building blocks are derived from their respective time-domain relationships.

PFD-CP: The PFD-CP has a linear range of +/-2π radians as depicted in the transfer characteristic shown in Figure 2-3. The charge pump outputs a maximum current of I_{CP} for a phase error magnitude of 2π radians. The transfer function of the PFD-CP in the linear range is given by:

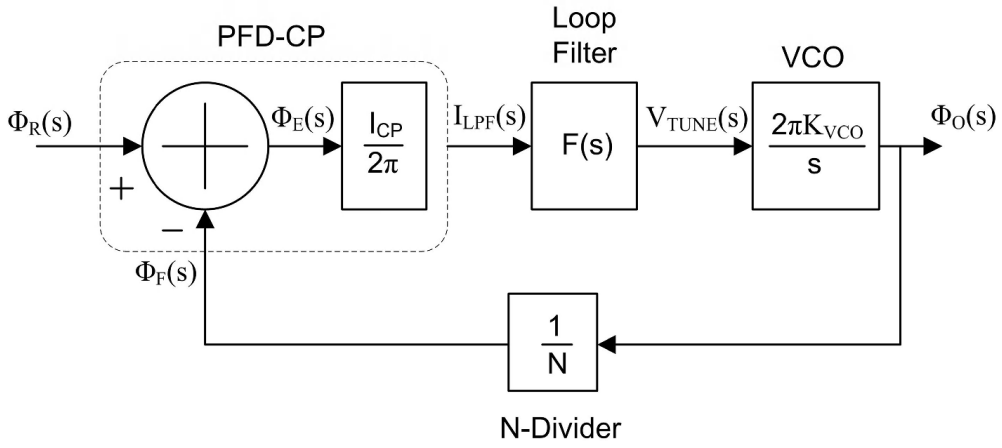

Figure 2-2 Linear Model of Synthesizer

$$\frac{I_{LPF}(s)}{\Theta_E(s)} = \frac{I_{CP}}{2\pi} \tag{2-2}$$

Loop Filter: A generic transfer function F(s) is used in Figure 2-2. Possible choices for F(s) will be considered in Section 2-3.

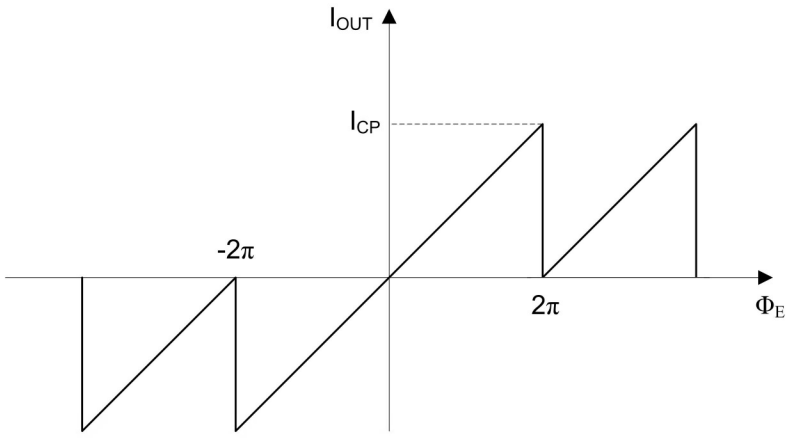

Figure 2-3 PFD Transfer Characteristic

$$\frac{V_{TUNE}(s)}{I_{LPF}(s)} = F(s) \tag{2-3}$$

VCO: The VCO frequency is related to the control voltage V_{TUNE} by the tuning sensitivity K_{VCO}.

$$\omega_O = 2\pi K_{VCO} V_{TUNE}$$

Equivalent phase relationship in S-domain is obtained as follows:

$$\frac{\Theta(s)}{V_{TUNE}(s)} = \frac{\omega_O(s)/s}{V_{TUNE}(s)} = \frac{2\pi K_{VCO}}{s} \tag{2-4}$$

N-Divider: Since phase is the time integral of frequency, the transfer function can be written as

$$\frac{\Theta_F(s)}{\Theta_O(s)} = \frac{1}{N} \tag{2-5}$$

Using the linear model, the synthesizer can be analyzed using the traditional feedback control theory. The closed loop transfer function relating the output phase Θ_O to the input phase Θ_R is given by:

$$H(s) = \frac{\Theta_O(s)}{\Theta_R(s)} = \frac{I_{CP} F(s) K_{VCO}}{s + \frac{I_{CP} F(s) K_{VCO}}{N}} \tag{2-6}$$

The loop gain transfer function G(s) is useful in analyzing the loop stability.

$$G(s) = H(s)\,|_{OPEN}\,\frac{1}{N} = \frac{I_{CP}F(s)K_{VCO}}{Ns} \tag{2-7}$$

Another useful transfer function relates phase error Θ_E to the input phase:

$$\frac{\Theta_E(s)}{\Theta_R(s)} = \frac{s}{s + \frac{I_{CP}F(s)K_{VCO}}{N}} \tag{2-8}$$

2.3. Loop Type and Order

With reference to the above transfer functions, the Type and order of the loop are defined as follows:

Type: refers to the number of poles at the origin in the loop gain transfer function G(s)

Order: refers to the highest power of S in the denominator of the closed-loop transfer function H(s).

It can be deduced from (2-6) and (2-7) that the loop filter transfer function F(s) determines the Type and order of the loop. Several choices for F(s) are possible leading to different loop' characteristics. In the following Sections, some of these characteristics are studied leading to the choice of a Type-II third-order loop.

2.3.1 Steady-State Error

The phase-error transfer function given by (2-8) can be used to compute the steady-state error in response to a frequency step at the reference input.

A frequency step of Δf_R can be represented in S-domain in terms of the reference phase input as

$$\Theta_R(s) = \frac{\Delta f_R}{s^2} \tag{2-9}$$

From (2-8), the phase error is

$$\Theta_E(s) = \frac{s}{s + \frac{I_{CP}F(s)K_{VCO}}{N}} \frac{\Delta f_R}{s^2} \tag{2-10}$$

From (2-10), the steady-state error can be obtained using the Final-value Theorem.

$$\begin{aligned} \underbrace{\lim}_{t\to\infty} \theta_E(t) &= \underbrace{\lim}_{s\to 0} s\Theta_E(s) \\ &= \frac{N\Delta f_R}{I_{CP}F(0)K_{VCO}} \end{aligned} \tag{2-11}$$

Equation (2-11) shows the dependency of the steady-state error on the dc gain F(0) of the loop filter. For zero steady-state error, F(0) has to be infinite which requires a pole in the loop filter at the origin. This results in a Type-II loop since the loop gain transfer function G(s) now has two poles at the origin (Equation (2-7)).

2.3.2 Stability

The magnitude response of the loop gain transfer function of the Type-II loop described above will have a slope of –12dB/octave at the cross over frequency (loop bandwidth), which leads to an unstable system unless a zero (lead network) is added to the loop filter that will result in a slope of –6dB/octave at the cross over frequency. However, for high-frequency noise filtering, 6dB/octave attenuation is insufficient in most practical cases. Addition of another pole increases the attenuation to 12dB/octave at frequencies much higher than the loop bandwidth. The result is a Type-II third-order loop with a loop filter transfer function of the form

$$F(s) = K \frac{\left(\frac{s}{2\pi f_Z} + 1\right)}{s\left(\frac{s}{2\pi f_P} + 1\right)} \tag{2-12}$$

K is the loop filter gain; f_Z and f_P are the zero and pole frequencies respectively. A common implementation of F(s) suitable for synthesizers using a PFD-CP combination is shown in Figure 2-4.

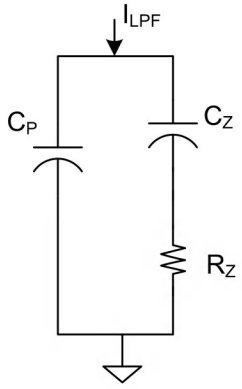

Figure 2-4 Common Loop Filter Implementation

For this loop filter

$$f_Z = \frac{1}{2\pi R_Z C_Z}; \qquad f_P = \frac{(C_Z + C_P)}{2\pi R_Z C_Z C_P}; \qquad K = \frac{1}{(C_Z + C_P)} \tag{2-13}$$

2.4. Maximum Phase Margin Loop

The Type-II third-order loop can be designed to have the maximum phase margin possible for given loop filter zero and pole frequencies. This is referred to as a maximum-phase-margin loop. Its loop bandwidth lies at the geometrical average of the zero and pole frequencies as will be demonstrated in this Section. The synthesizer implemented in this work uses the maximum-phase-margin loop, which is a common choice and has a well-defined loop-design procedure. Useful relations for the loop design are derived in this Section.

Consider once again the loop gain transfer function of a Type-II third-order loop in the frequency domain.

$$G(j2\pi f) = -\frac{I_{CP} K_{VCO}}{N(2\pi f)^2} \frac{1}{(C_Z + C_P)} \frac{(1 + j f / f_P)}{(1 + j f / f_Z)} \tag{2-14}$$

Its phase response is given by:

$$\Psi(j2\pi f) = -\pi + \arctan(f/f_Z) - \arctan(f/f_P) \tag{2-15}$$

The frequency f_{MAX} at which the phase is maximum, can be found by setting the derivative of $\Psi(j2\pi f)$ to zero. The result is shown in (2-16).

$$f_{MAX} = \sqrt{f_Z f_P} \tag{2-16}$$

In order to have the maximum phase margin, the phase of $G(j2\pi f)$ at the cross-over frequency (the loop bandwidth f_C) should be maximum as shown in Figure 2-5. This implies the loop bandwidth f_C should be set to f_{MAX} which is the geometrical average of the zero and pole frequencies.

$$f_C = f_{MAX} = \sqrt{f_Z f_P} \tag{2-17}$$

The value of the maximum phase margin Φ_{MAX} can be found using (2-15) and (2-17). Letting $\alpha = f_P/f_Z$

$$\Phi_{MAX} = \arctan\left(\frac{\alpha - 1}{2\sqrt{\alpha}}\right) \tag{2-18}$$

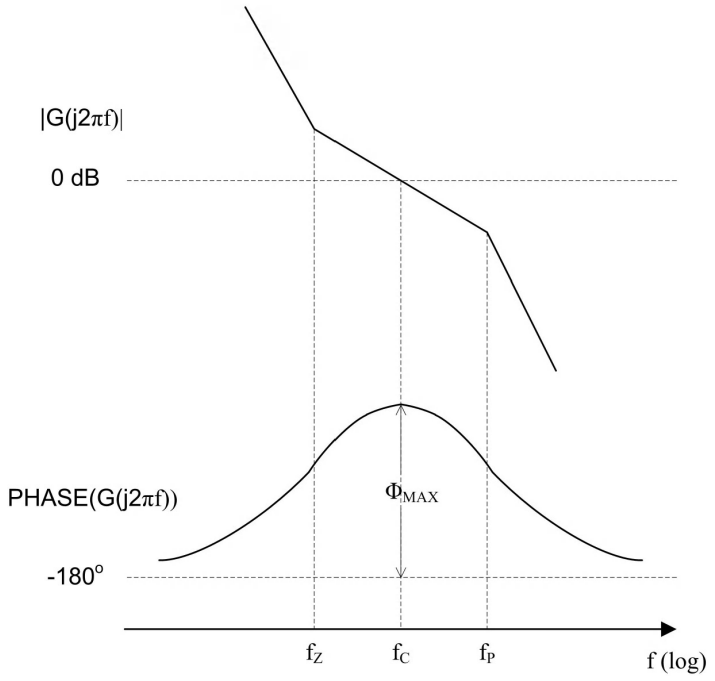

Figure 2-5 Magnitude and Phase Response of Maximum Phase Margin Loop

In turn α can be expressed as a function of Φ_{MAX}.

$$\alpha = \frac{1}{\left(-\tan\left(\Phi_{MAX}\right)+1/\cos\left(\Phi_{MAX}\right)\right)^2} \tag{2-19}$$

The expression for loop bandwidth can now be derived by setting $|G(j\pi f)| = 1$ and using (2-17). After simplification the following expression for f_C is obtained.

$$f_C = \frac{I_{CP}K_{VCO}R_Z}{2\pi N}\frac{C_Z}{\left(C_Z + C_P\right)} \tag{2-20}$$

The loop filter zero and pole frequencies in terms of f_C and α are given by:

$$f_Z = \frac{f_C}{\sqrt{\alpha}}; f_P = \sqrt{\alpha} f_C \tag{2-21}$$

Thus the maximum-phase-margin loop has a greatly simplified loop design procedure. With the specified system-level parameters, equations (2-17) to (2-21) can be used for loop design as described in Section 4.3.

CHAPTER 3. TRADE-0FF AND PROPOSED SOLUTION

In the design of PLL frequency synthesizers, there exists a trade off between the switching time and spur level at the output [1] [2] both of which are strongly dependent on the loop bandwidth. Though theory allows a maximum of 1/10 of the reference frequency for the loop bandwidth [3], practically the bandwidth is several orders of magnitude smaller than this limit in order to meet the spurious performance requirement. Further in Integer-N synthesizers, the reference frequency cannot exceed the channel spacing. These limitations result in elongated switching times for conventional Integer-N synthesizers. In this Chapter, this trade-off is analyzed in terms of the loop parameters and an existing solution and its limitations are presented before proposing a modified solution that overcomes these limitations.

3.1. The Trade-Off

Some of the closed-form expressions used in this discussion are based on an approximation of a third-order loop with a second-order loop, since the analysis of the former is cumbersome and unrewarding in the context of understanding the trade-off. Consider the maximum-phase-margin loop of Section 2.4 with a damping ratio $\varsigma < 1$. The open loop bandwidth f_C is derived in Section 2.4 and is a function of the loop parameters as shown in (3-1).

$$f_C = \frac{I_{CP} K_{VCO} R_Z}{2\pi N} \frac{C_Z}{(C_Z + C_P)} \tag{3-1}$$

Reference spurs at the output are caused due to several non-idealities. One such non-ideal effect, the charge pump leakage is considered in this discussion. Charge pump leakage I_{LEAK} results in a phase offset ϕ_E between the PFD inputs given by:

$$\phi_E = 2\pi \frac{I_{LEAK}}{I_{CP}} \tag{3-2}$$

The phase offset gives rise to a spur at the output of magnitude approximately given by [4]:

$$P_R[dBc] = 20\log\left(\frac{1}{\sqrt{2}}\frac{\frac{I_{CP}R_Z}{2\pi}\phi_E K_{VCO}}{f_R}\right) - 20\log\left(\frac{f_R}{f_P}\right)$$
$$= 20\log\left(\frac{1}{\sqrt{2}}\frac{f_C}{f_R}N\phi_E\right) - 20\log\left(\frac{f_R}{f_P}\right) \quad (3\text{-}3)$$

The closed form expression for the switching time of a third-order loop is not well defined. Hence an approximation based on a second-order loop is used which provides sufficient insight into the trade-off. The switching time is determined by the natural frequency and damping factor which are defined in (3-4).

$$\omega_N = \sqrt{\frac{I_{CP}K_{VCO}}{N(C_Z + C_P)}} = 2\pi\sqrt{f_C f_Z}$$
$$\varsigma = \frac{1}{2}\frac{\omega_N}{2\pi f_Z} = \frac{1}{2}\sqrt{\frac{f_C}{f_Z}} \quad (3\text{-}4)$$

The switching time for a frequency step Δf_O and settling error tolerance ε is given by [5]:

$$t_s \cong \frac{\ln\left(\frac{\Delta f_O}{\varepsilon\sqrt{1-\varsigma^2}}\right)}{\omega_N\varsigma} = \frac{\ln\left(\frac{\Delta f_O}{\varepsilon\sqrt{1-\varsigma^2}}\right)}{\left(2\pi f_C/2\right)}; \quad (3\text{-}5)$$

From (3-3) and (3-5) it follows that the loop bandwidth limits are set by:

- Minimum limit – Switching time requirement
- Theoretical maximum limit – 1/10 of reference frequency (f_R)
- Much lower maximum limit – Spurious performance requirement

Thus a trade-off exists, a common solution to which is to use an adaptive bandwidth synthesizer as described in the following section.

3.2. Existing Solution

In the adaptive bandwidth approach, high loop bandwidth is used during frequency steps and the loop bandwidth is restored to its nominal value after the frequency has settled to its new value so the switching time and spurious requirements can both be met to an acceptable level [6] [7]. The following section discusses the basic principle in detail.

3.2.1 Basic Principle of Adaptive Bandwidth Synthesizer

From (3-5) it can be seen that the switching time for a given frequency step and error tolerance depends on the loop bandwidth f_C and the damping factor ς. Note that the switching time can also be expressed in terms of the change in the VCO control voltage corresponding to the frequency step Δf_O in which case the frequency error tolerance ε will be replaced with the equivalent control voltage error tolerance. The VCO tuning sensitivity K_{VCO} relates the equivalent parameters in the two expressions.

Equation (3-5) suggests that to reduce the switching time by a factor of β, the loop bandwidth has to be increased by a factor of β while keeping the damping factor constant. In terms of the loop parameters this is equivalent to increasing the charge pump current I_{CP} by a factor of β^2 and reducing the loop filter resistor R_Z by a factor of β. Even though spurious requirements limit the loop bandwidth to be narrower, it can be made wider during the locking process and then restored after lock is established. This is the basic principle of operation of the adaptive bandwidth synthesizer shown in Figure 3-1. The 'locked' signal generated by a lock-detect circuit not shown, or a predetermined timing signal is utilized for the adaptive bandwidth control.

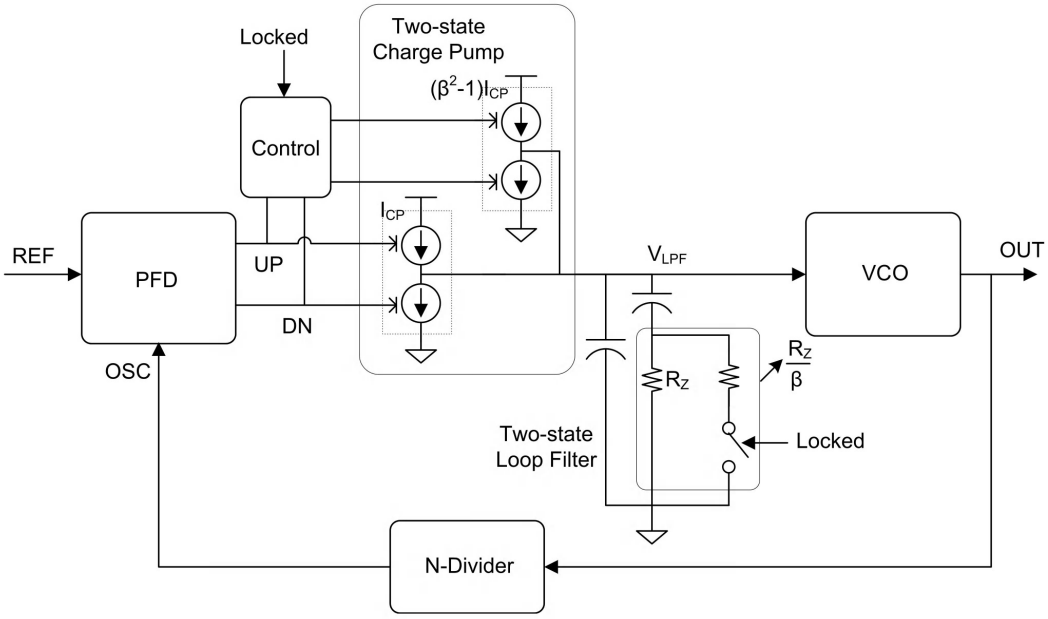

Figure 3-1 Adaptive Bandwidth Architecture

3.2.2 Limitation of Existing Solution

The adaptive system described above can be employed to achieve significant improvement in the switching time. The switching of bandwidth is accomplished by switching an element in the loop filter usually a resistor. If the synthesizer has to settle to a very small frequency error (< 1ppm) in a very short time (tens of microseconds), it becomes important to make the transition from high bandwidth to low bandwidth as smooth as possible; otherwise the glitches arising from switching of bandwidth contribute significantly to the overall switching time [6] [7]. An applicable case is the synthesizer used in a GSM base station transmitter, which has a switching time specification of less than 10μs for a frequency jump of 75MHz with 0.1ppm error tolerance. It is thus important to limit the level of secondary glitches when switching from high bandwidth to low bandwidth mode. The sources of the secondary glitches are the parasitic capacitances associated with the switch element (typically a MOS switch). At the time of frequency step, the switch in Figure 3-1 is closed to reduce the effective resistance in the loop filter by a factor β. When frequency step

is complete the switch has to be opened to restore the bandwidth. The transitions on the voltage signal controlling the on/off states of the MOS switch cause glitches on the control voltage line. The size of the parasitic gate-drain capacitance of the MOS switch determines among other things, the level of these glitches. If the control voltage has already settled to within the tolerance window at the time of turning off the MOS switch, then the glitches can cause the control voltage to swing outside of the window, thus increasing the overall switching time of the synthesizer.

3.3. Proposed Solution

As described in Section 3.2, minimizing the gate-drain capacitance of the MOS switch helps to restrict the level of glitches to within the tolerance window. A second factor that determines how fast the VCO control voltage settles after a glitch occurs is the effective bandwidth after switching. Thus if a relatively large MOS switch is used to switch from high bandwidth to nominal bandwidth, then the size of the MOS switch and the narrow bandwidth after switching together contribute to a significantly large switching time.

The solution proposed in this thesis is based on multi-step bandwidth switching. Here the bandwidth is restored to the nominal value in several steps using charge pump and loop filter resistor arrays as shown in Figure 3-2. By using smaller steps from high bandwidth to nominal bandwidth, the secondary glitches can be effectively controlled due to two main factors. First, if the MOS switch resistance is a fixed fraction of the resistor it switches then it can be shown mathematically that the maximum MOS switch size in the multi-step approach is less than the size of the single MOS switch used in the one-step approach. Secondly, transients caused by turning off MOS switches at each of the steps have to settle down with a larger bandwidth compared to the one-step approach, which also helps to reduce the overall switching time. The above claims are supported through behavioral simulations described in Section 3.4.

To keep the optimal damping factor constant and only increase the loop bandwidth the following relationship has be valid at each of the bandwidth steps.

$$\sqrt{I_{CP}}R_Z = \text{Constant} \tag{3-6}$$

Thus a given sequence of bandwidth steps $\beta_H f_L \rightarrow \beta_1 f_L \rightarrow \beta_2 f_L \rightarrow \ldots \rightarrow f_L$ (f_L – low bandwidth, $\beta_H f_L (= f_H)$ – high bandwidth; $\beta_H > \beta_1 > \beta_2 > \ldots > 1$) requires the following sequence of R_Z and I_{cp} steps:

$$R_Z/\beta_H \rightarrow R_Z/\beta 1 \rightarrow R_Z/\beta 2 \rightarrow \ldots. \rightarrow R_Z \tag{3-7}$$
$$\beta_H{}^2 I_{cp} \rightarrow \beta_1{}^2 I_{cp} \rightarrow \beta_2{}^2 I_{cp} \rightarrow \ldots. \rightarrow I_{cp}$$

One of the factors determining the effectiveness of the proposed scheme is the pattern used for the steps since it determines the sizes of the switches used in the loop filter. There are several possibilities such as binary stepping of I_{CP}, linear stepping of I_{CP} or the Fibonacci pattern for I_{CP}. Binary stepping and the Fibonacci pattern result in successive bandwidths being close to each other near the nominal bandwidth and far apart near the high bandwidth, with the switch sizes decreasing with decreasing bandwidth. Linear stepping of bandwidth results in equal-sized MOS switches and can also be an optimum choice. Though the different patterns were simulated, the results are presented in Section 3.4 only for the binary pattern. Note that once the high bandwidth and the type of pattern are chosen, the number of steps will be fixed. For example if the high bandwidth is eight times the nominal bandwidth and if binary stepping of I_{CP} is chosen, then the number of steps will be six corresponding to I_{CP} multipliers of 64, 32, 16, 8, 4, 2, 1. The second factor determining effectiveness is the time at which each step occurs which is pre-determined based on the initial lock time in the high bandwidth mode, the magnitude of perturbation at each step, and the effective bandwidth at the start of each step. In the two-step case presented in Section 3.4, the time for the next step is chosen to be the time of the first zero crossing of the control voltage in the

current step. +/- 15% variations in the time steps have also been considered to demonstrate the robustness of the proposed scheme.

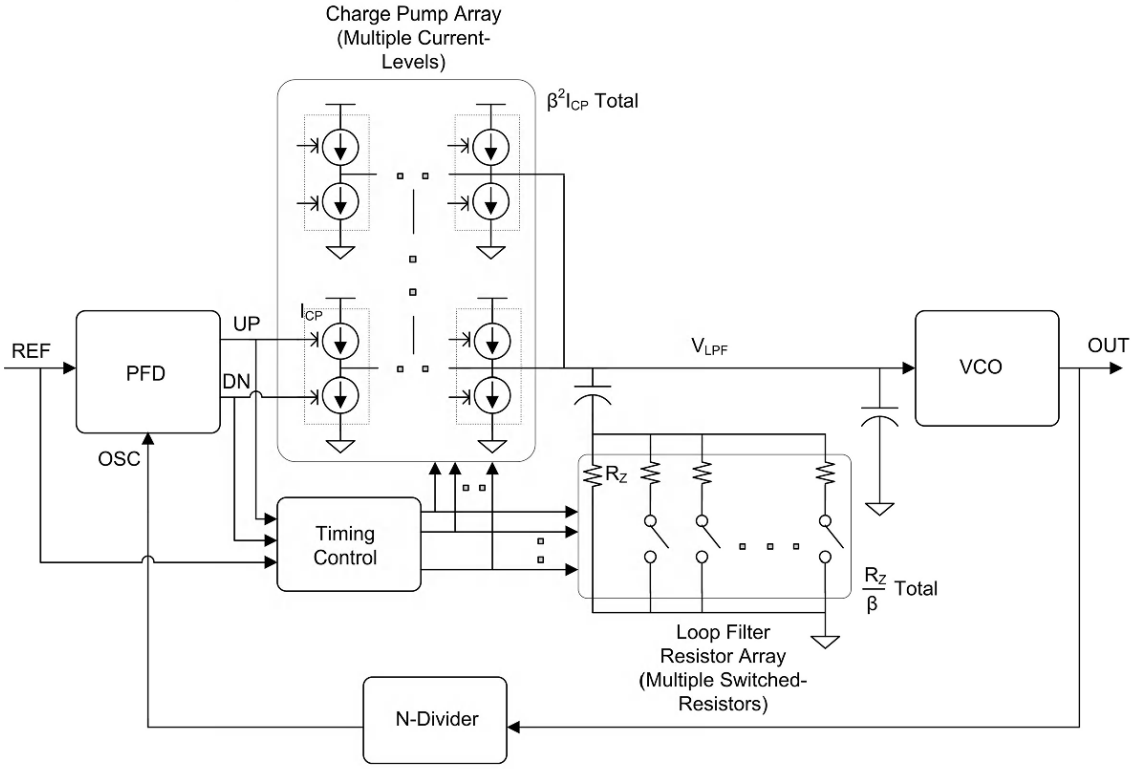

Figure 3-2 Proposed Adaptive Bandwidth Architecture

3.4. Behavioral Simulation

3.4.1 GSM Fractional-N Synthesizer

The proposed scheme is first verified through behavioral simulation of a Fractional-N (output frequency is a fractional multiple of reference frequency) synthesizer using GSM specifications. The reference frequency can be much higher than the channel spacing for Fractional-N synthesizers, hence the loop bandwidth limit is mainly set by the spurious requirements. The objective of this simulation is to demonstrate the level of improvement that can be achieved with the proposed scheme in synthesizers with very stringent switching time specifications. The simulation setup uses behavioral models for all the building blocks

including the programmable charge pump except the loop filter, which uses NMOS switches so that the effect of secondary glitches can be simulated. The loop filter configurations used in the one-step and two-step cases are shown in Figure 3-3. In all the branches of the switched-resistor-array, containing a fixed resistor and a MOS switch, the on-resistance of the switch is always chosen to be 1/9 of the fixed resistance. The loop parameters used in the simulation are given in Table 3-1.

Table 3-1 Behavioral Simulation Parameters for GSM Synthesizer

Frequency step Δf_O	75MHz (1710MHz – 1785MHz)
Error tolerance ε	0.1ppm
Reference frequency f_R	26MHz
Nominal charge pump current I_{CP}	0.213mA
Nominal loop bandwidth f_C	40KHz
High loop bandwidth $8f_C$	320KHz
Phase margin Φ_M	46.4^o
Damping factor ς	0.7906
Nominal loop filter resistor R_Z	2.5KΩ
Loop filter zero f_Z	16KHz
Loop filter pole f_P	100KHz
VCO tuning sensitivity K_{VCO}	37.5MHz/V

Firstly, comparison is done between the switching times obtained in the following two cases.

Case1: High bandwidth switched to nominal bandwidth in one step

$8f_C \rightarrow f_C$

Case2: High bandwidth switched to nominal bandwidth in two steps

$8f_C \rightarrow \sqrt{8}\, f_C \rightarrow f_C$

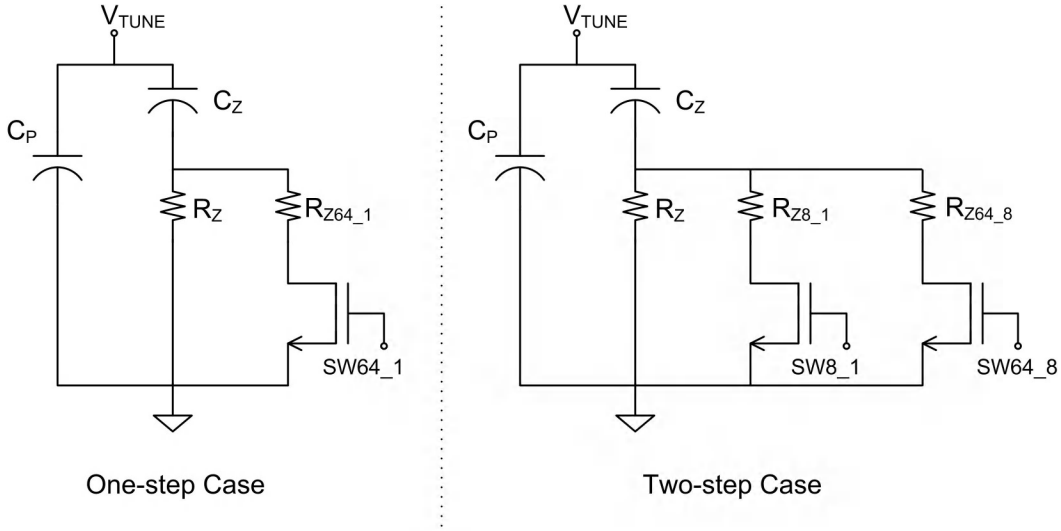

Figure 3-3 Loop Filter Configurations for One-step and Two-step Bandwidth Switching

In the one-step case, the bandwidth is switched at 10.5μs (using initial lock time estimate) whereas in the two-step case, the first step occurs at 10.5μs and the second at 11.43μs. Figure 3-4 shows the locking profile where the VCO control voltage settling to the tolerance window is shown against time. The total switching time is 18.21μs for the one-step case and 11.75μs for the two-step case. This is nearly 35% improvement in the switching time.

It was mentioned in Section 3.3 that the time at which switching of bandwidths has to occur is determined based on the zero-crossings of the tune voltage. To demonstrate robustness of the proposed scheme, simulations are performed with +/- 15% variations in these times. Table 3-1 shows the results of these simulations. It can be observed that with the variations included, there is still a 35% improvement in the total switching time.

Finally, a synthesizer with six bandwidth steps is simulated. The first step occurs at 8.1µs (optimal for six bandwidth steps) and time between subsequent steps is 0.5µs. Loop filter in this case uses six switched- resistors similar to the configuration shown in Figure 3-3. The I_{CP} and R_Z at each step are multiplied by factors as shown below:

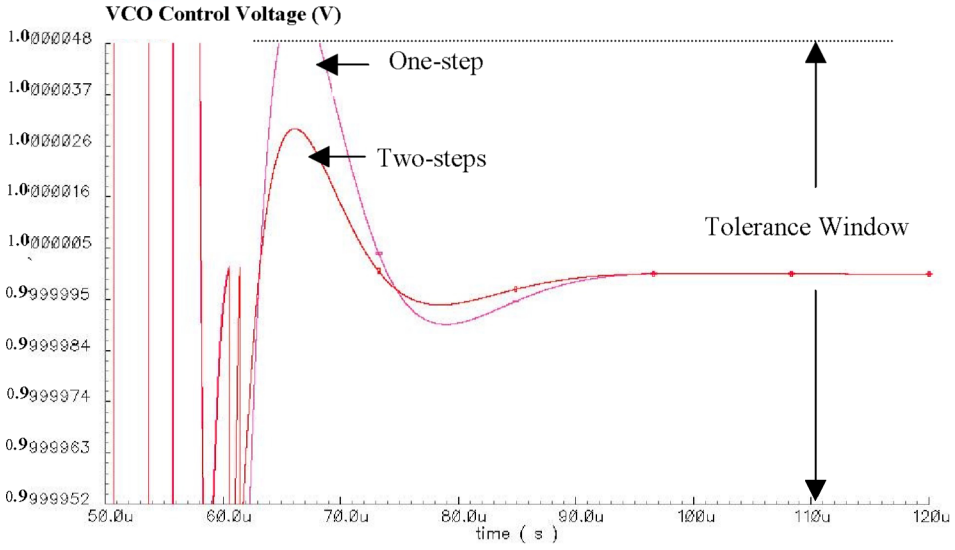

Figure 3-4 Locking Profile for One-step and Two-step GSM Synthesizer

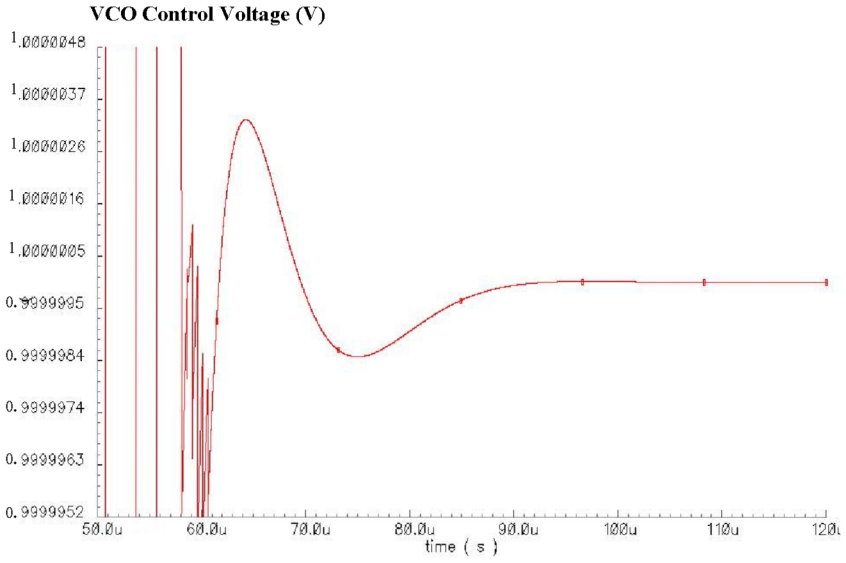

Figure 3-5 Locking Profile for Six-step GSM Synthesizer

I_{CP} multiplier: 64 → 32 → 16 → 8 → 4 → 2 → 1

R_Z fraction: 1/8 → $1/\sqrt{32}$ → 1/4 → $1/\sqrt{8}$ → 1/2 → $1/\sqrt{2}$ → 1

Locking profile is shown in Figure 3-5. The total switching time in this case is 10.62µs.

Table 3-2 Total Switching Time with 15% Variation in Bandwidth Intervals

One step – at t_{SW1}		**Two steps - first step at t_{SW1} and second step at t_{SW2}**		
t_{SW1} (µs)	**Total switching time t_{SW} (µs)**	**t_{SW1} (µs)**	**t_{SW2} (µs)**	**Total switching time t_{SW} (µs)**
10.15	18.21	10.5	11.43	11.75
			11.29	11.84
			11.57	11.67
10.14	18.46	10.14	11.43	11.43
			11.29	11.29
			11.57	11.57
10.36	19.11	10.36	11.43	11.52
			11.29	11.61
			11.57	11.57

3.4.2 Integer-N Synthesizer with Tight Error Tolerance

Next a 2.4GHz Integer-N synthesizer with an error tolerance of 1ppm for an 80MHz step is considered. Simulations are performed to study the advantage of the proposed multi-step bandwidth-switching scheme in terms of the achievable switching times when the loop

bandwidth is limited by both the reference frequency and the spurious requirements. Table 3-3 shows the simulation parameters.

Table 3-3 Behavioral Simulation Parameters for Integer-N Synthesizer

Frequency step Δf_O	80MHz (2400MHz – 2480MHz)
Error tolerance, ε	1ppm
Reference frequency f_R	1.172MHz
Nominal charge pump current I_{CP}	28μA
Nominal loop bandwidth f_C	10kHz
High loop bandwidth $4f_C$	40kHz
Phase margin Φ_M	46.4^o
Damping factor ς	0.7906
Nominal loop filter resistor R_Z	54.7kΩ
Loop filter zero f_Z	4kHz
Loop filter pole f_P	25kHz
VCO tuning sensitivity K_{VCO}	100MHz/V

The locking profile (Figure 3-6) shows a 25% improvement in switching time with four bandwidth steps (total switching time = 68.8μs) versus one bandwidth step (total switching time = 92.2μs).

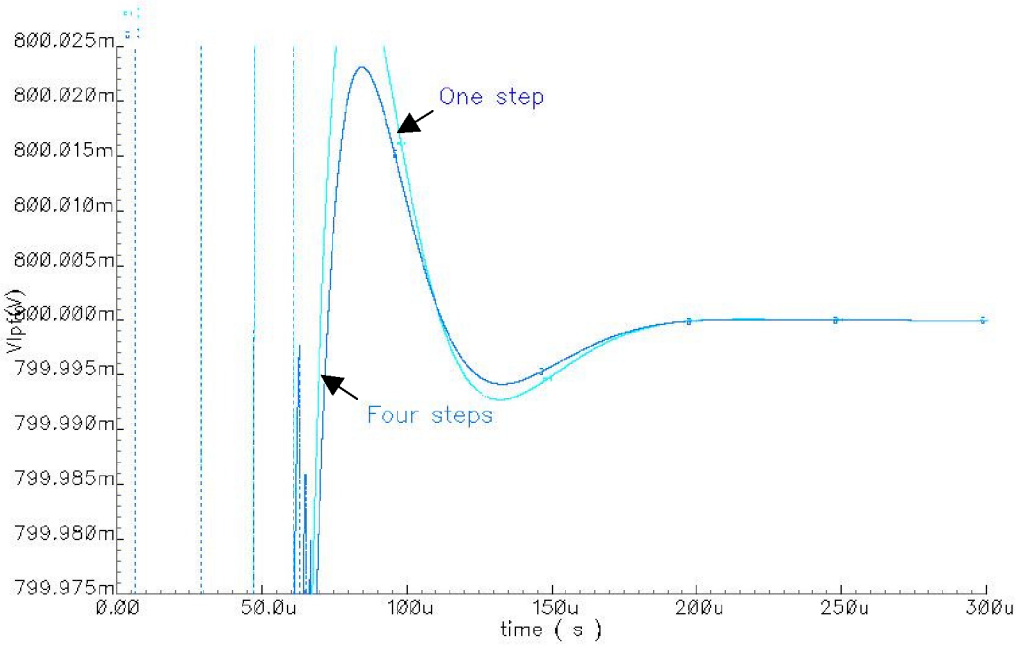

Figure 3-6 Locking profile for One-step and Four-step Integer-N Synthesizer

The above behavioral simulations substantiate the effectiveness of the proposed multi-step bandwidth-switching scheme. This simple and practical on-chip solution is implemented on silicon in a 2.4GHz Integer-N synthesizer, design of which is described in extensive detail in Chapters 4 and 5.

CHAPTER 4. SYSTEM DESIGN

In this Chapter, the system-level implementation of the proposed adaptive bandwidth synthesizer is discussed. Details of the implemented architecture and the system-level parameters are presented and the design specifications for the individual blocks are derived based on these parameters.

4.1. Architectural Implementation

The proposed architecture uses a Type-II third-order loop similar to the conventional architecture. However, to implement multi-step bandwidth switching, the charge pump and the loop filter of the conventional synthesizer are modified as illustrated in Figure 3-2. The charge pump is implemented as an array of multiple unit cells that provides programmable current and the loop filter resistor is implemented as a switched-resistor array. The unit cells in the charge pump array and the resistors in the switched-resistor array are controlled with timing signals generated by a control block such that the sequence shown in Equation (3-7) is followed. For implementing on silicon, a realistic value of $\beta_H = 4$ is used with binary stepping of I_{CP}. This results in four bandwidth steps with the high to nominal bandwidth sequence as shown in (4-1).

$$4f_C \rightarrow 2\sqrt{2}\, f_C \rightarrow 2f_C \rightarrow \sqrt{2}\, f_C \rightarrow f_C \qquad (4\text{-}1)$$

The proposed architecture requires a timing control block, which ensures that each bandwidth setting is valid for a preset number of clock cycles starting from the instant when frequency jump is initiated. Additionally, in contrast to the conventional architecture, the implemented architecture uses a fixed ratio divider instead of a programmable divider and a multiplexer for selecting reference clock inputs for the following reasons. Typically in a synthesizer, the instant when frequency step is initiated corresponds to the change in the division ratio of the N-Divider. However, to reduce design time and complexity and focus primarily on the proposed bandwidth-switching scheme, only a fixed ratio divider is used in

the new architecture. To achieve frequency step with a fixed ratio divider, a multiplexer (hereby referred to as reference multiplexer) is used to select between two reference clocks, which differ in frequency by an amount corresponding to the VCO frequency step. This way, frequency step is initiated by a change in the state of the multiplexer select signal f_{STEP}. Assume for example, that the two input clocks to the multiplexer have frequencies, f_{R1} = 1MHz and f_{R2} = 1.2MHz. If the select input changes from '0' to '1', it causes a reference frequency step of 200 KHz, which causes the VCO frequency to jump from 2.048GHz to 2.4576GHz (with divider ratio fixed at 2048).

Before concluding this section, it should be mentioned that in addition to the four-step mode, the proposed architecture also supports single step and non-adaptive modes, used mainly for comparison of switching times.

4.2. Bandwidth Switching Sequence

In the previous section, the role of the control block was briefly mentioned. In this Section the function of the control block is put into perspective by looking at the sequence of events that occur during the frequency switching process in the four-step mode. The sequence is illustrated in the timing diagram of Figure 4-1.

1. Reference multiplexer select input f_{STEP} changes state indicating a frequency step from f_{R1} to f_{R2} or vice versa, where f_{R1} and f_{R2} are the frequencies of the two reference clock inputs.
2. Immediately, the control signals SW16_8, SW8_4, SW4_2 and SW2_1 go high thereby activating all the unit cells in the charge pump array and all the resistors in the loop filter resistor array. This is the highest bandwidth mode of the synthesizer with four times the nominal bandwidth f_C. With $4f_C$ bandwidth, the loop responds quickly to the frequency step by adjusting the VCO control voltage. The significant

amount of the required change in VCO control voltage is achieved in this mode while the lesser bandwidth modes are used for finer settling.

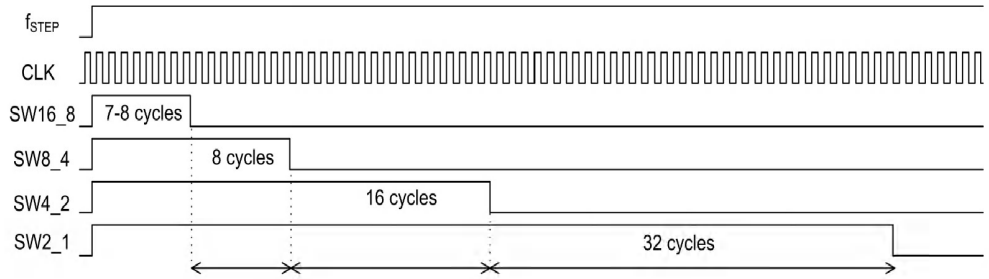

Figure 4-1 Timing Diagram of Bandwidth Switching Sequence

3. The high bandwidth mode should not be retained for a long time as this can cause significant peaking in the VCO control voltage and result in undesired behavior. The duration of the high bandwidth in this architecture is set to between seven and eight clock cycles. After this duration, $2\sqrt{2}\,f_C$ bandwidth mode starts, i.e., SW16_8 is made low while other control signals remain high. With the new bandwidth, the control voltage further settles to the final value.
4. In this manner each bandwidth mode remains for a fixed number of clock-cycles before next bandwidth modes starts as per the sequence shown in (4-1).
5. Finally after all control signals are low, nominal bandwidth is restored. The switching time is measured from the transition on f_{STEP} until the control voltage settles to a tolerance window around its final value.

The control block is thus very essential for the proposed synthesizer architecture.

4.3. Loop Design

Before proceeding with the design of individual blocks, the loop parameters are calculated based on the system-level specifications. The specified and the derived parameters

are described in detail in the context of the step-by-step loop design procedure given below. A Type-II third-order maximum-phase-margin loop described in Section 2.4 is used.

Step 1: The nominal loop bandwidth is specified based on the theoretical limit. With reference frequency f_R of 1.172MHz, the theoretical limit for the loop bandwidth is 117.2kHz. A value of f_C = 10kHz is chosen such that enough margin is available for the highest bandwidth mode. Note that in practice f_C is chosen based on spurious requirement, however goal of this design is only to compare switching times for a given nominal f_C, hence no spurious requirement is specified.

Step 2: As discussed in [6], for minimum switching time, phase margin Φ_M around 50^o is required. From (2-18), a value of α = 6.25 gives a phase margin of 46.4^o. This sets the damping factor ς to 0.7906 (Equation (3-4)).

Step 3: With the nominal loop bandwidth and damping factor known, the switching time in the non-adaptive mode can be derived using (3-5) for given frequency step and error tolerance. For a 20MHz step (2.4GHz to 2.42GHz) and 30ppm error, the switching time is 195μs. Note that this is only an approximate theoretical value. The simulated and/or measured value will be used as the basis for the improvement in the switching time in the four-step mode.

Step 4: For the maximum-phase-margin loop, the ratios of the loop bandwidth to the loop filter zero and pole frequencies are given by (2-21). With α = 6.25, the zero and pole frequencies are respectively f_Z = 4kHz and f_P = 25kHz.

Step 5: If the VCO tuning sensitivity K_{VCO} is known, Equation (3-1) can be used to calculate the product $[I_{CP}R_Z]$. The tuning sensitivity of monolithic VCOs varies significantly over process corners and temperature. This causes the open loop bandwidth also to be process-corner and temperature dependent. To overcome this dependency, in some advanced implementations, the charge

pump current I_{CP} is designed to track the variations in K_{VCO}. However only a simpler implementation is used in this work. A specified K_{VCO} value of 70MHz/V is used in Equation (3-1) to calculate the product $[I_{CP}R_Z]$.

Step 6: Next, the nominal charge pump current I_{CP} or the loop filter resistor R_Z are specified. Smaller I_{CP} requires larger R_Z and vice versa for a constant $[I_{CP}R_Z]$. With large R_Z, smaller capacitors can be used in the loop filter thus saving die area. A value of nominal $I_{CP} = 40\mu A$ is found to give capacitor values that can be implemented in the available die area.

Step 7: With $I_{CP} = 40\mu A$, R_Z is found to be 54.7kΩ. For the zero and pole frequencies calculated in Step 4, C_Z and C_P are calculated to be 727pF and 138.5pF.

The circuit level implementation of the building blocks of the synthesizer using the calculated loop parameters is discussed in the following chapter. Table 4-1 summarizes the system specifications.

Table 4-1 System Specifications

Architecture	
Integer-N architecture Type-II third-order Loop Adaptive bandwidth High bandwidth four times nominal bandwidth Four steps from high-to-nominal bandwidth Binary stepping of charge pump current	
Top-Level Specifications	
Output frequency	2.4GHz
Reference frequency	1.172MHz
Divider ratio	2048 (fixed)
Loop Parameters	
Specified	**Derived**
f_C = 10kHz	t_{SW} = 195μs (Δf_O = 20MHz; ε = 72.6kHz)
$\Phi_M = 46.9^o$	ς = 0.7906 C_Z/C_P = 5.25 f_Z = 4kHz f_P = 25kHz
K_{VCO} = 70MHz/V	$[I_{CP}R_Z]$ = 2.188V
I_{CP} = 40μA	R_Z = 54.7kΩ C_Z = 727pF C_P = 138.5pF

CHAPTER 5. DESIGN OF BUILDING BLOCKS

In this Chapter, circuit level implementation of various building blocks of the synthesizer is discussed. The design specifications are based on the loop parameters calculated in Section 4.3. The simulated performance of these building blocks and the whole synthesizer is presented in Chapter 6.

5.1. Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) provides the output signal of the frequency synthesizer. By controlling the output frequency with the phase-frequency error signal generated through feedback, the VCO can be made to 'lock' to a stable reference clock. Different types of VCOs exist, however in communication systems where spectral purity is important, a LC VCO is preferred since the frequency can be accurately set by using resonance of the LC tank while a negative resistance in the form of cross-coupled active device pair compensates for the losses in the tank. In these types of VCOs, frequency control can be achieved using variable capacitors or varactors.

5.1.1 VCO Analysis

Before presenting specific details of circuit design, the basic design equations and trade-offs are reviewed.

Figure 5-1 shows the conceptual implementation of a LC oscillator with an ideal negative conductance element g_{mN}. R_{PEQ} represents combined losses in the tank that includes the series losses of L and C and additional loss due to interconnects.

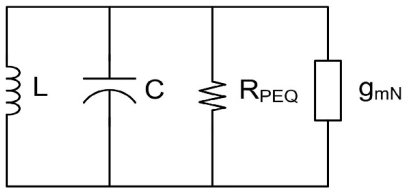

Figure 5-1 Conceptual LC Oscillator

The negative conductance compensates the tank losses and sustains oscillations at the resonance frequency of the tank [8],

$$\omega_O = \frac{1}{\sqrt{LC}} \tag{5-1}$$

The characteristic impedance (Z_O) and quality factor (Q) at the resonant frequency ω_O are important properties of the LC tank that directly affect the VCO performance and are given by

$$Z_O = \left(\frac{1}{\omega_O C}\right) = \omega_O L = \sqrt{\frac{L}{C}} \tag{5-2}$$

$$Q = \frac{R_{PEQ}}{Z_O} \tag{5-3}$$

The necessary minimal conductance to sustain oscillations is given by:

$$g_{mN} = \frac{1}{R_{PEQ}} = \frac{1}{QZ_O} \tag{5-4}$$

However, in reality, to enable startup under all conditions, R_N is over designed by a factor $\alpha > 1$ such that $g_{mN} = \alpha \frac{1}{R_{PEQ}}$

Fig. 5-2 shows the implementation of LC oscillator using PMOS cross-coupled pair as the negative conductance element. It can be shown that the PMOS cross-coupled pair provides a negative conductance of

$$g_{mN} = \frac{g_{m1}}{2} \tag{5-5}$$

In (5-5), g_{m1} (= g_{m2}) is the transconductance of M_1 (M_2) given by (5-6) with I_T being the tail current.

$$g_{m1} = \sqrt{\mu_p C_{ox} \frac{W_1}{L_1} I_T} \tag{5-6}$$

Thus for a given oscillation frequency ω_O, startup gain α and power consumption I_T, the device sizes can be computed using (5-4), (5-5) and (5-6).

$$\frac{W_1}{L_1} = \frac{4\alpha^2}{(QZ_O)^2 \mu_p C_{ox} I_T} \tag{5-7}$$

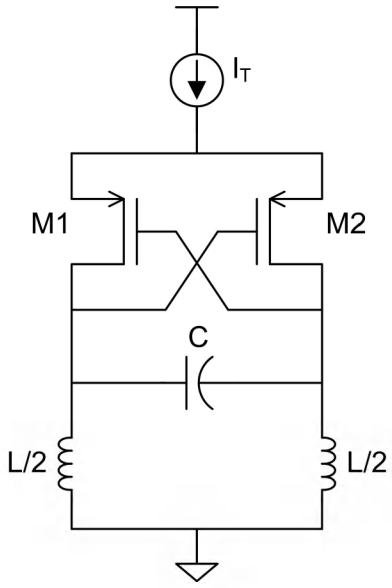

Figure 5-2 PMOS Implementation of Negative Conductance

Equations (5-1) and (5-7) provide basic constraints for the VCO design apart from the tunability requirements described in Section 5.1.3. The process technology used (TSMC 0.25μm) imposes further constraints on the choice of L and C and the achievable quality factor Q. Specific details of the VCO design tailored to the TMSC 0.25μm process are given in the following section.

5.1.2 VCO Design

The TSMC 0.25μm mixed-mode process offers thick top metal (physical thickness: 1.5μm) that can be used to build on-chip spiral inductors. The process design kit (PDK) supplied by the vendor includes a device library for active and passive devices. For inductors, the library offers selectable number of turns from 2.5 to 6.5. Once the number of turns is selected, the inductance is fixed. For the differential VCO design, two inductors of 5.5 turns each were selected based on the desired oscillation frequency and available die area. An inductor with 5.5 turns gives an inductance of about 8.675nH and has a Q of 7.3 @2GHz.

With the value of L known, the desired tank capacitance can be found from (5-1). As mentioned before, varactors, also from the device library, are used. The varactors structure

consists of a NMOS array on N-well. The actual varactor capacitance in the operating range of the VCO is much less than the value predicted by (5-1), considering the parasitic capacitances of the PMOS devices and the loading of the coarse tuning capacitors described in Section 5.1.3

The final design of the VCO core is shown in Figure 5-3. It should be mentioned that the design equations presented above serve only as a starting point while a thorough simulation using different model corners and temperatures is used to arrive at the design shown in Figure 5-3. A tail current of 2mA is chosen for reasonable power consumption and is found to give sufficient start up gain. A current mirror driven by off-chip resistor supplies the tail current.

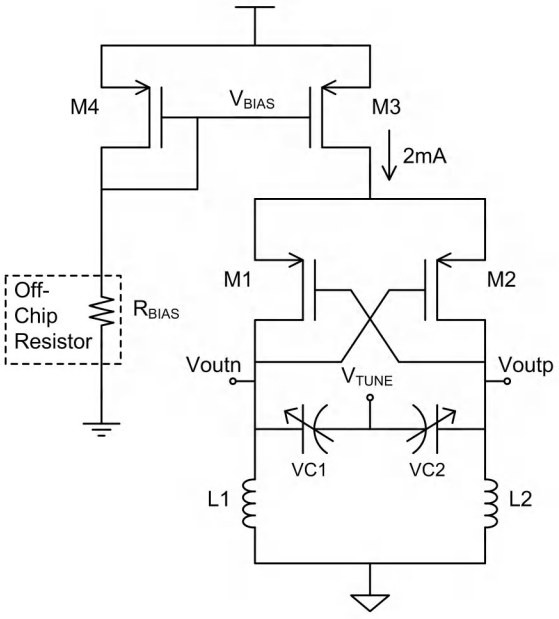

Figure 5-3 VCO Core

5.1.3 Tunability

In integrated LC oscillators, the tuning range is limited by two main factors. One is the range of the control voltage V_{TUNE}, which is limited to within at least 500mV of the positive and ground rails. With 2.5V charge pump supply this translates to only 1.5V or with

3.3V charge pump supply as is used in the current design, it translates to 2.3V. The limited range may be insufficient for the application at hand, given the large variations in center frequency caused by on-chip components. Second factor is the need to use a VCO with a small tuning sensitivity (K_{VCO}). This is important because higher K_{VCO} means any noise voltage present at the tuning port of the VCO causes frequency modulation of the VCO output and degrades its phase noise.

For these reasons practical on-chip VCOs are always complemented with discrete or coarse tuning. By providing three to four bits of programmability of the center frequency, the process variations can be accounted for in a discrete manner. The VCO uses four bits as shown in Figure 5-4, with each successive bit doubling the tank capacitance.

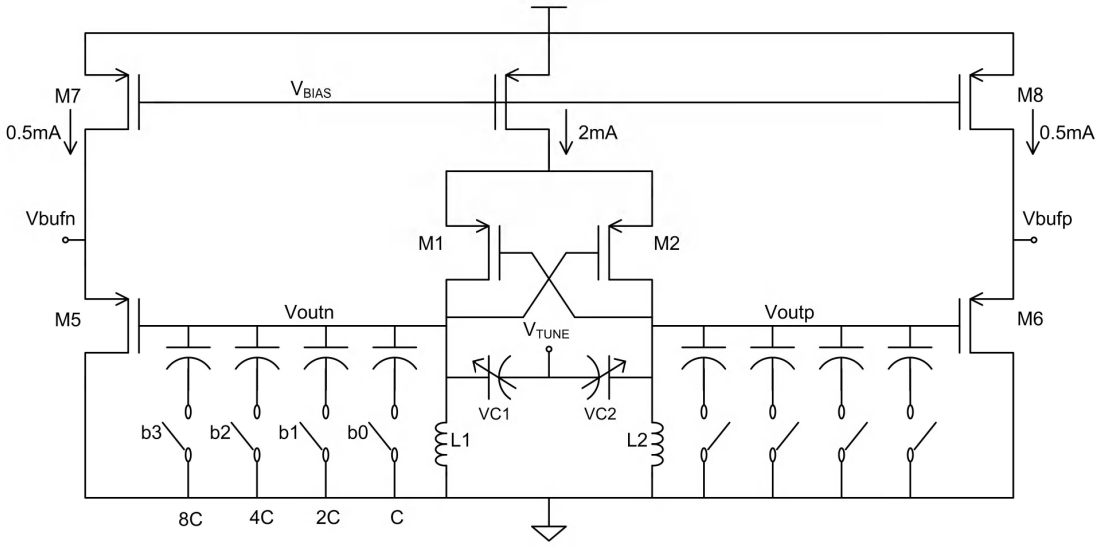

Figure 5-4 VCO with Coarse Tuning and Output Buffers

5.1.4 Output Buffers

The interface of the VCO with the divider is complicated due to the differences in the dc-levels and signal swings at the VCO output and the divider input. The VCO core produces

differential outputs centered on a zero dc level (In the absence of special biasing, the inductors force the dc operating point to zero). However, the high-speed divider that follows the VCO is based on source coupled logic (SCL) which operates on minimal signal swings to enable faster rise and fall times. The divider requires clock input of 600mVpp with a dc level of 1.9V. Thus PMOS level-shifters are employed at the outputs of the VCO core as shown in Figure 5-4. The devices M5 and M6 shift the dc level of the VCO outputs while also reducing the signal swing according to the current flowing in M7 and M8 respectively. An average current of 500μA is consumed by each level-shifter with the peak current as high as 1mA. The high frequency nature of the VCO output necessitates such high current consumption.

5.2. Charge Pump

The charge pump converts the UP and DN pulses from the PFD into equivalent source and sink currents for the loop filter. The proposed architecture uses a 16-cell charge pump array for programmable current. In the following sections, the design of the charge pump unit cell and the implementation of the charge pump using multiple unit cells are described.

5.2.1 Design Considerations

An ideal charge pump must have zero mismatch of the UP and DN currents and infinite output impedance. Several factors affect the UP and DN current mismatch including the accuracy of the reference current and the mismatch of the current mirrors used in the charge pump. To achieve high output impedance, a cascode current mirror can be used at the output. A low-voltage cascode is preferable, since it maximizes the available V_{TUNE} range. In addition to using a low voltage cascode, dedicated power supply to the charge pump that is higher than the power supply of the other synthesizer blocks helps to increase the V_{TUNE} range further. Modern CMOS processes typically offer the option of "thick-oxide" transistors

that can be used in high volt applications. For example, in the TSMC 0.25μm process, the nominal supply voltage is 2.5V whereas 3.3V supply can be used with the thick-oxide transistors.

Before presenting details about the circuit design of the charge pump, the dead-zone phenomenon, which is critical to the design of the PFD and the charge pump, is discussed. The current sources in the charge pump are constantly turned-on and off in response to the UP and DN pulses from the PFD. A narrow UP or DN pulse may not sufficiently turn-on the current source owing to the parasitic capacitances at various nodes inside the charge pump. Since the width of the UP and DN pulses is determined by the phase difference of the PFD inputs, a phase difference less than a finite value +/-Φ_D doesn't produce an equivalent charge pump output current. The +/- Φ_D interval is known as the dead-zone of the PFD-CP.

Dead-zone is undesirable since during this interval the loop is essentially open causing the VCO to be free running and pick up any noise on the control line without feedback correction. Thus a smaller dead-zone is preferable for a low-noise synthesizer. The charge pump used in this work however has large (~20ns) dead-zone due to the slow cascode current mirrors used for high output impedance and better isolation between the switching nodes and output node. Dead-zone is eliminated by producing minimum UP and DN pulses instead of a 'no-pulse' for zero phase difference. The width of the minimum pulses is set by the PFD as explained in Section 5.3

5.2.2 Charge Pump Cell Design

As mentioned in Section 4.1, the adaptive bandwidth synthesizer uses a charge pump with multi-step programmable current. The maximum programmable current is 16 times the current during normal operation. To achieve this programmability, the charge pump is designed as an array of 16 identical cells. Each cell outputs a nominal current of 40μA. One

unit cell is always operating, while the remaining 15 cells operate only when the synthesizer is switching to a new frequency. A timing control block described later in Section 5.6 controls the operation of these 15 cells. The design of the charge pump unit cell is described in detail below.

The charge pump cell converts UP and DN pulses from the PFD into UP (sourcing) and DN (sinking) current pulses. This is accomplished using current steering switches and low voltage cascode mirrors. The magnitude of the current pulses is the charge pump current I_{CP} that is set to 40μA as specified in Section 4.3. Shown in Figure 5-5, is the portion of the charge pump cell that generates the DN current I_{DN}. UP current is generated by the complementary version of the circuit shown in Figure 5-5. The current steering switches M1, M2 driven by complementary signals DN, DNb steer the tail current $I_{REF,DN}$ either to the low voltage cascode current mirror (M5-M9) or to ground in the presence and absence of the DN pulse respectively. The current steered to the cascode mirror is then reflected at the output V_{LPF} with a mirror ratio of four.

It can be seen that the current in the cascode mirror goes to zero in the absence of the DN pulse. This causes the current mirror to turn-off rather slowly compared to the turn-on phase. In order to speed up the turn-off response, a standby current is added. The standby current is usually a small fraction of the full current and doesn't affect the loop filter current I_{LPF}. The standby current is added through another pair of current steering switches M3, M4 used to steer the standby current $I_{SBY,DN}$. $I_{SBY,DN}$ acts as secondary tail current. When the primary tail current is steered to ground, the standby current is steered to the current mirror and vice versa. This ensures the current mirror always carries a finite current and thus responds faster to the UP and DN pulse transitions. The charge pump uses a $I_{SBY,DN}$ of 2μA and $I_{REF,DN}$ of 12μA.

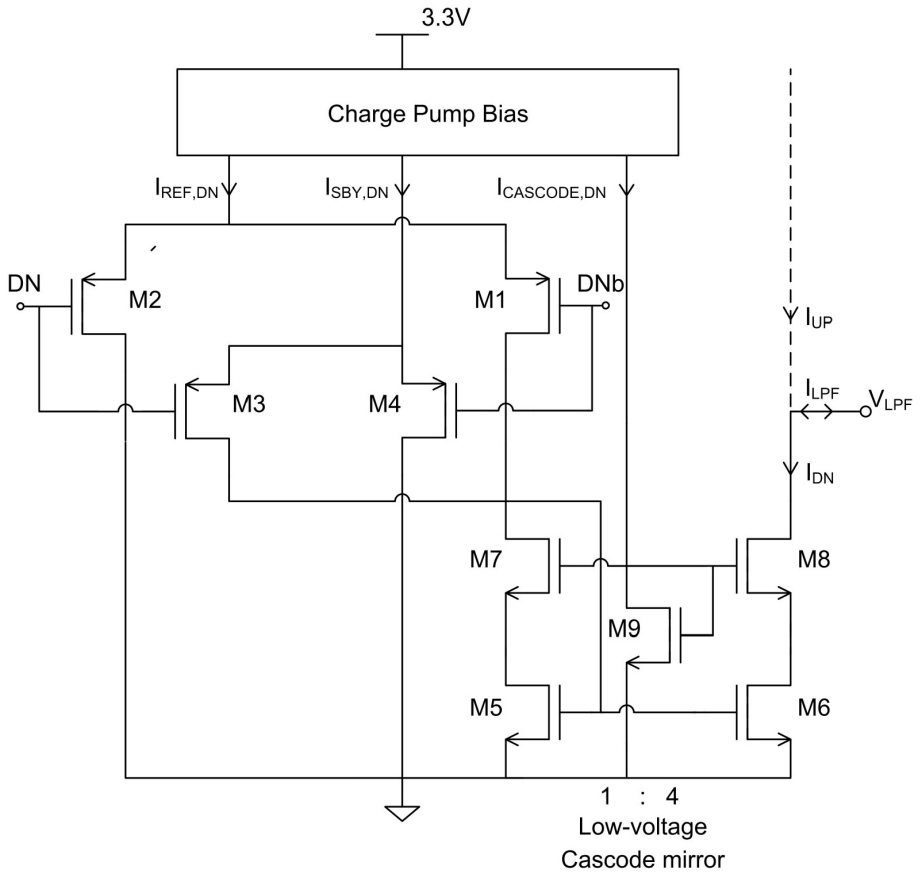

Figure 5-5 Part of Charge Pump Cell Generating Down Current

The advantage of using a low voltage cascode is the reduction in the minimum value of V_{LPF} required for M5-M8 to remain in saturation. Note that V_{LPF} is essentially the VCO control voltage V_{TUNE} and thus maximizing the range of V_{LPF} is equivalent to increasing the tuning range of the VCO. Up to one threshold voltage reduction in the minimum value of V_{LPF} can be achieved with the low-voltage cascode leading to significant improvement in the VCO tuning range.

A 3.3V supply is used for the charge pump to further maximize the V_{LPF} range. Accordingly thick-oxide transistors are used everywhere except for the current steering devices M1-M4 since the gates of these devices are controlled by UP and DN signals which are in the 2.5V domain.

5.2.3 Charge Pump Bias

The accuracy of the charge pump current is very important to the performance of the synthesizer. Specifically, the reference current source that is used to generate the output current of the charge pump should be accurate to few ppm over process corners and temperature. This is accomplished typically by an on-chip band-gap reference. However, an on-chip reference has not been used in this work and the reference current is set using an external resistor R_{CPBIAS} (Figure 5-6). Each unit cell uses 4μA bias current and the V_{LPF} nodes of all the 16 cells are tied together so that 64μA current is needed through R_{CPBIAS}.

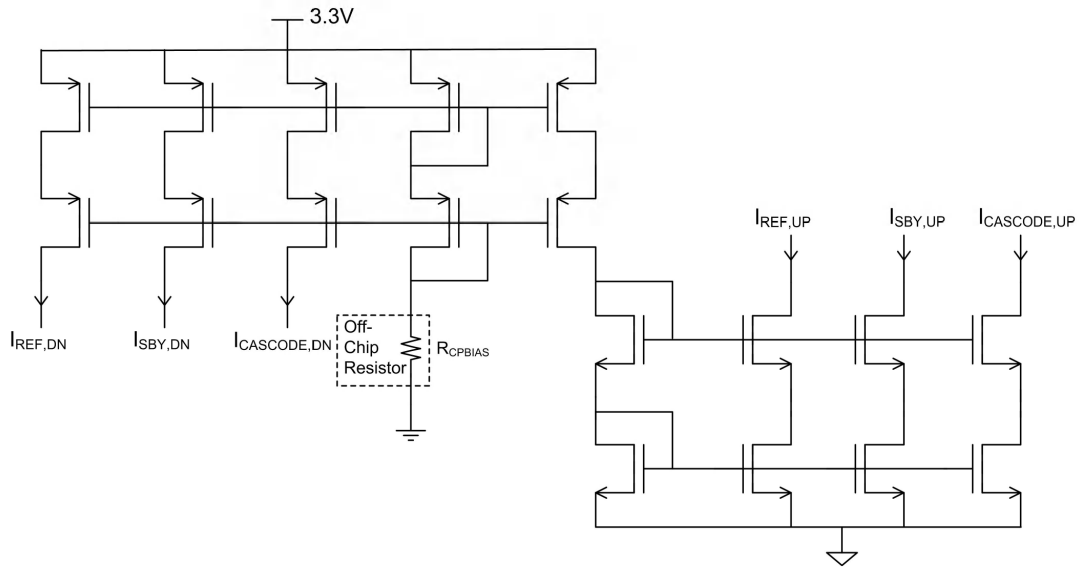

Figure 5-6 Charge Pump Bias Circuit

5.2.4 Charge Pump Array

Using the single charge pump cell, a 16-cell charge pump array shown in Figure 5-7 is created. Gated logic controls the operation of 15 unit cells using the control signals from the timing control block. For the single cell that is always on, the standby current always flows, whereas for the remaining 15 cells, standby is turned off altogether once the frequency

switching is complete This is to reduce disturbance in steady state at the V_{LPF} node where currents from all the 16 cells are summed.

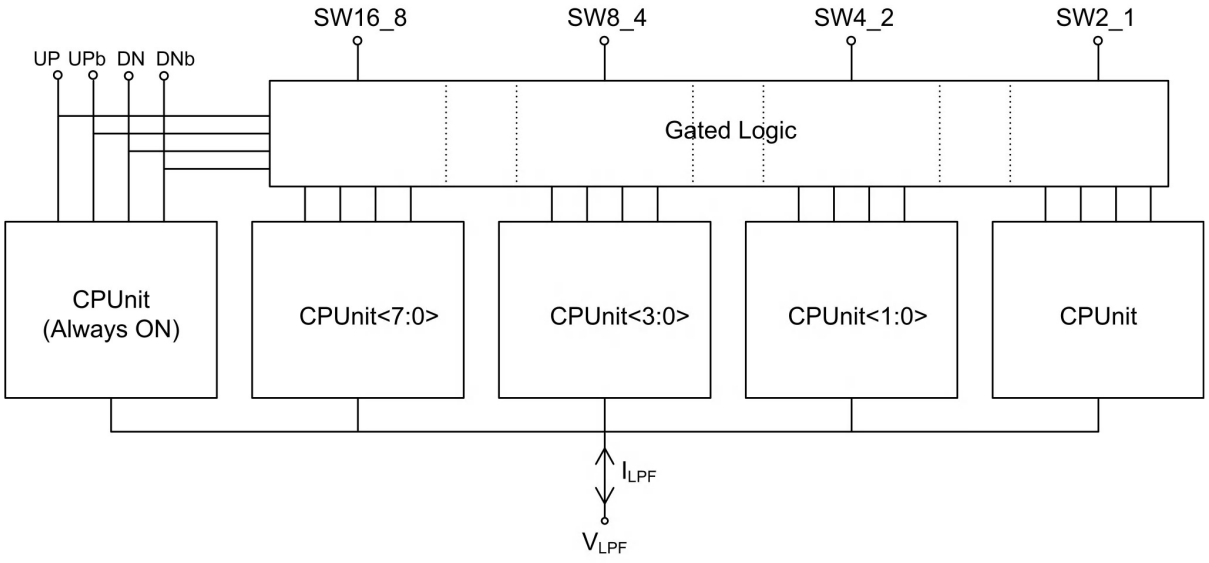

Figure 5-7 16-cell Charge Pump Array

5.3. Phase Frequency Detector (PFD)

Conventional D-Flip Flop (DFF) based PFD is used. Figure 5-8 shows the gate level implementation of the PFD. The internal reset (RSTi) is activated when both UP and DN outputs are high, but after a finite delay to eliminate the dead zone. As explained in Section 5.2.1, this delay is determined based on the response time of the charge pump.

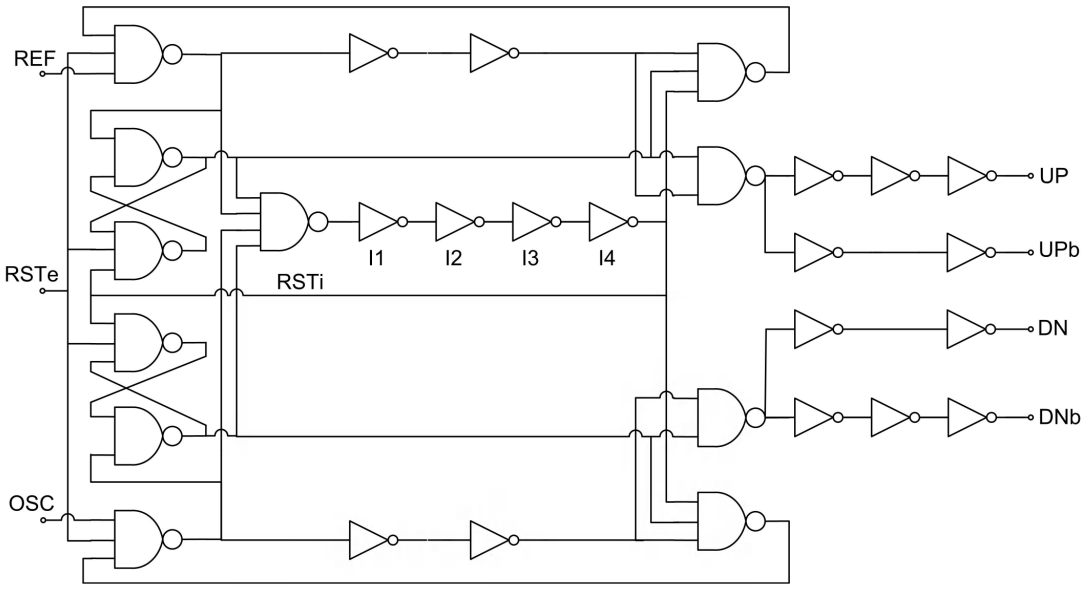

Figure 5-8 Phase Frequency Detector

The reset delay is achieved using a chain of long channel inverters (I1 – I4). To generate complementary signals, cascades of inverters are used at the outputs such that UP, UPb, DN and DNb are closely matched in terms of delay from inputs REF and OSC. The external reset (RSTe) is used to initialize the DFF outputs on power up.

5.4. Loop Filter (LPF)

A second-order passive loop filter is used. The values of R_Z, C_Z and C_P are calculated in Section 4.3 and are shown in Table 5-1. In order to have programmable loop bandwidth, R_Z is implemented as a resistor array consisting of a fixed resistor R_Z in parallel with four switched resistors R_{Z16_8}, R_{Z8_4}, R_{Z4_2} and R_{Z2_1} as shown in Figure 5-10. During normal operation all the NMOS switches are OFF so that the total resistance is R_Z and the nominal bandwidth is f_C. As higher bandwidth is needed during a frequency jump, the NMOS switches are turned ON and then OFF in a sequence determined by the timing control block. With all switches ON, the total resistance is $R_Z/4$ and the loop bandwidth is $4f_C$. The switched-resistor values are chosen such that at any bandwidth setting Equation (3-8) is

satisfied. The resistance of the NMOS switch is chosen to be 1/9 of the resistor it switches. The fifth resistor R_{Z16_1} is used in the single-step mode to switch the bandwidth from $4f_C$ to f_C in one-step.

Table 5-1 Loop Filter Parameters

R_Z	54.7kΩ
C_Z	727pF
C_P	138.5pF

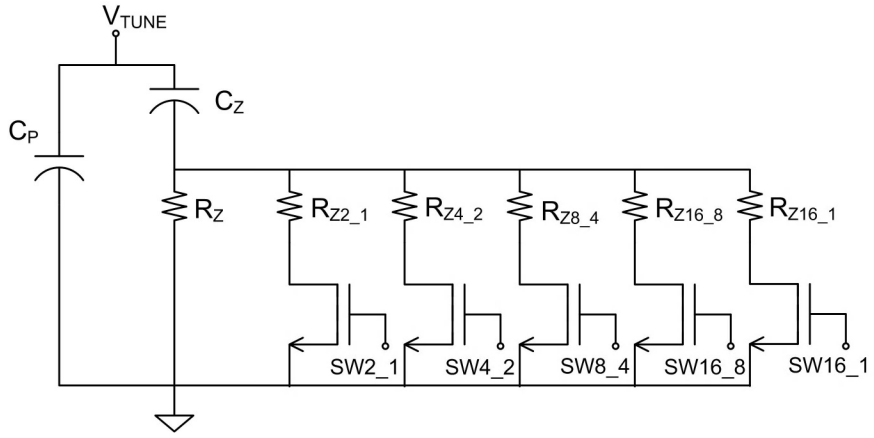

Figure 5-9 Loop Filter with Switched-Resistor Array

Metal-insulator-Metal (MiM) capacitors are readily available in the TSMC 0.25μm process. The MiM structure consists of a layer called CTM (Capacitor Top Metal) on top of Metal 4. These capacitors provide a capacitance density of $1fF/\mu m^2$. Large arrays of small unit capacitors are used for C_Z and C_P. P+ poly resistor without salicide has a sheet resistance of 160Ω/sq and is used to implement all the resistors in the loop filter.

5.5. N-Divider

The N-Divider is one of the power-hungry blocks in a synthesizer. High-power source-coupled logic (SCL) is needed to divide the high-frequency VCO output. SCL uses small swing signals and high supply current to achieve division of high frequency inputs. Since the frequency divides down with each stage, in practice, only the first three or four stages of the divider use SCL, followed by standard digital logic to implement further division. In this design, a divide-by-2048 block is implemented as a divide-by-8 SCL stage followed by a divide-by-256 digital stage. Before proceeding it should be mentioned once again that only a fixed-ratio divider is used in this work for reasons explained in Section 4.1.

Figure 5-10 shows the implementation of div-by-2048 block. Design of the divide-by-8 SCL stage (DIV_8_SCL) and the divide-by-256 digital stage (DIV_256_DIGITAL) is described below.

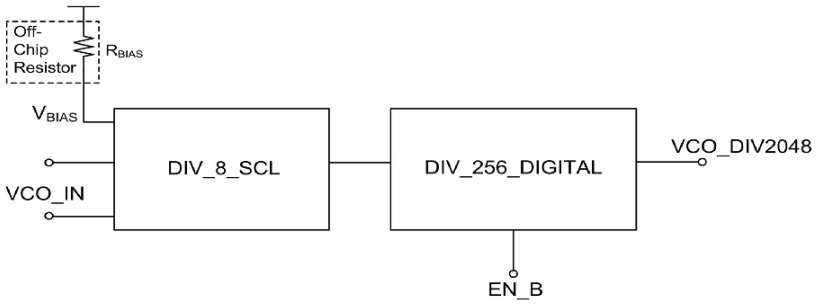

Figure 5-10 Top-level Implementation of N-Divider

5.5.1 Divide-by-8 SCL Divider

The basic element of the divide-by-8 SCL divider is a SCL D-Latch that forms a D flip-flop (DFF) in Master-Slave configuration. The DFF is in turn configured as a divide-by-2 stage (DIV_2_SCL) by connecting its outputs back to the inputs in a complementary fashion (Qb is connected to D and Q is connected to Db) as shown in Figure 5-11. Finally three divide-by-2 stages are cascaded to form the divide-by-8 stage.

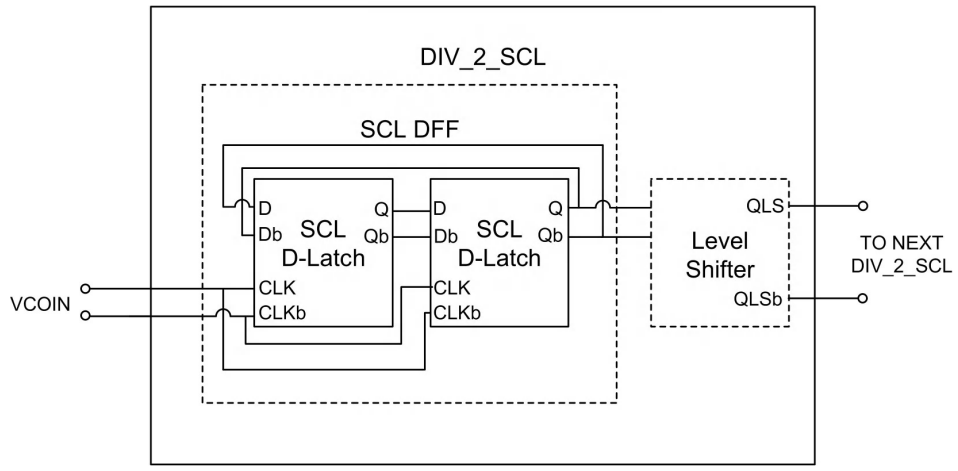

Figure 5-11 SCL DFF Configured as Div-by-2

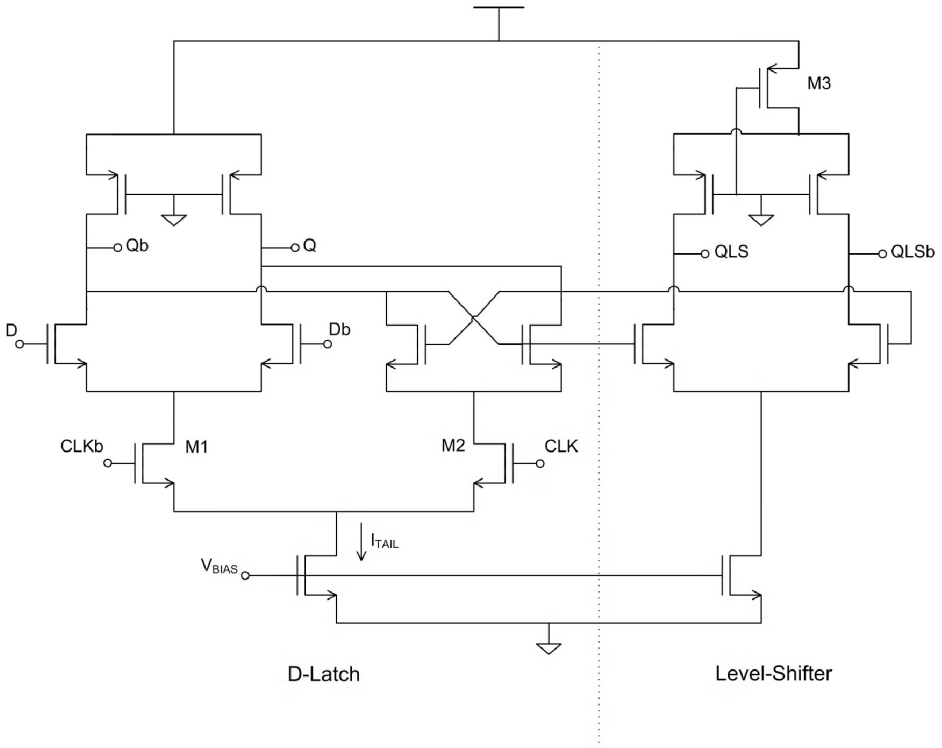

Figure 5-12 SCL D-Latch and Level-Shifter

Figure 5-12 shows the conventional SCL D-latch combined with the level-shifter circuit. M3 acts as the level-shifting resistor. A level-shifter is required because of the following signal swing requirements at the data (D), clock (CLK) inputs and the outputs (Q).

D: 1.9V – 2.5V; Q: 1.9V – 2.5V; CLK: 1.6V – 2.2V

Thus to connect the output of the first divide-by-2 to the input of the next divide-by-2, a 300mV shift in the dc level is required. The signal swings are kept to the minimum required to steer the tail current between M1 and M2. The first divide-by-2 stage operates on the highest frequency input and thus uses the maximum tail current of 100uA. As the frequency is divided down in subsequent stages, the tail current also can be reduced. Accordingly, the second and third divide-by-2 stages use only 50uA tail current. The third divide-by-2 is followed by differential to single-ended rail-to-rail converter shown in Figure 5-13. The differential stage amplifies the small swing signals such that they cross the threshold level of the inverter that follows it. The inverters convert the single-ended signal to a rail-to-rail logic signal suitable as input to the following divide-by-256 stage.

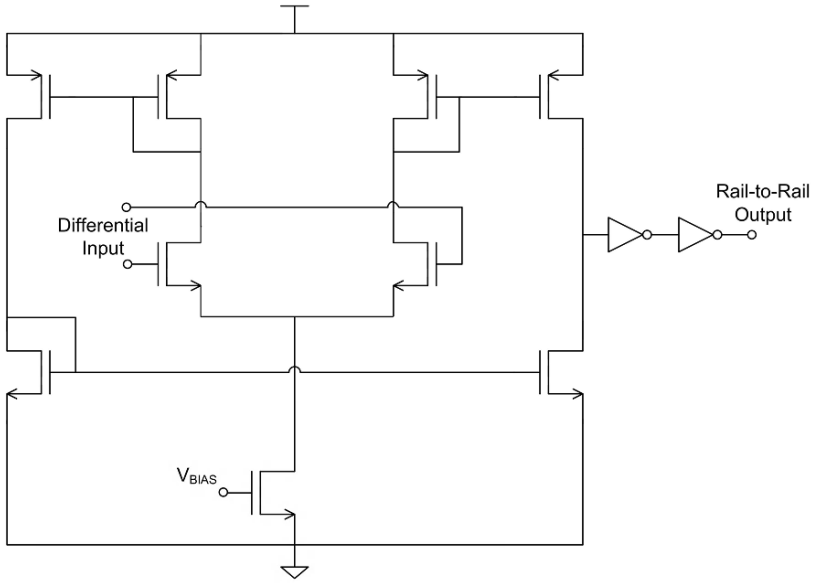

Figure 5-13 Differential to Singled-ended Converter

5.5.2 Divide-by-256 Digital Divider

Similar to the SCL divide-by-2 stage, a DFF implemented in static CMOS rail-to-rail logic can be used to build a digital divide-by-2 circuit. The advantage of using static CMOS

logic is that no static current is used and thus it gives a low power implementation. However, since rail-to-rail logic is used, only low frequency signals (< 500MHz) can be divided using this implementation.

Figure 5-14 shows the CMOS gate level implementation of the divide-by-2 circuit. The active-low enable (EN_B) acts like a reset on power up. The divide-by-256 circuit is simply a cascade of eight divide-by-2 stages.

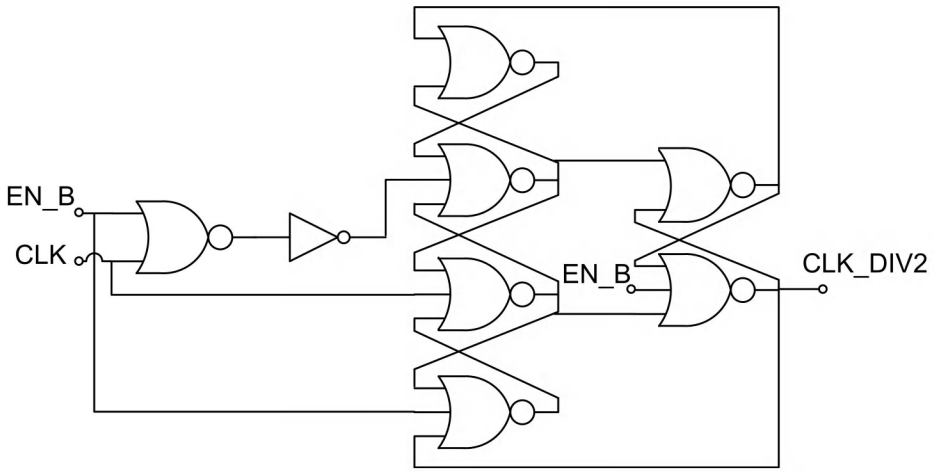

Figure 5-14 Digital Divide-by-2

5.6. Timing Control

Apart from the basic building blocks, the adaptive synthesizer uses a digital block to control the timing of the bandwidth steps. At the start of a frequency step indicated by the change in f_{STEP}, the bandwidth control signals (SW16_8, SW8_4, SW4_2 and SW2_1) are all activated. The de-activation of these signals follows a sequence as shown in the timing diagram in Figure 4-1. The reference clock for the synthesizer is also used as the reference clock for the timing control. It takes up to 64 clock cycles to restore the bandwidth from $4f_C$ to nominal.

The timing control also supports one-step mode. In this case, bandwidth is initially set to $4f_C$ and restored to nominal in a single step at the instant corresponding to the first step in

the four-step mode. Note that in the one-step mode, the control signal SW16_1 controls the switched resistor R_{Z16_1} while all other control signals are inactive.

Figure 5-15 shows the implementation of the timing control block. The multiplexer selects the controls outputs depending on mode select (one-step or four-step). The control signals are set by a transition in f_{STEP} and are reset by the outputs of the divide-by- 16, 32, 64 and 128 stages respectively for SW16_8, SW8_4, SW4_2 and SW2_1. The SW16_1 control signal in the one-step mode is the same as SW16_8 control signal in the four-step mode.

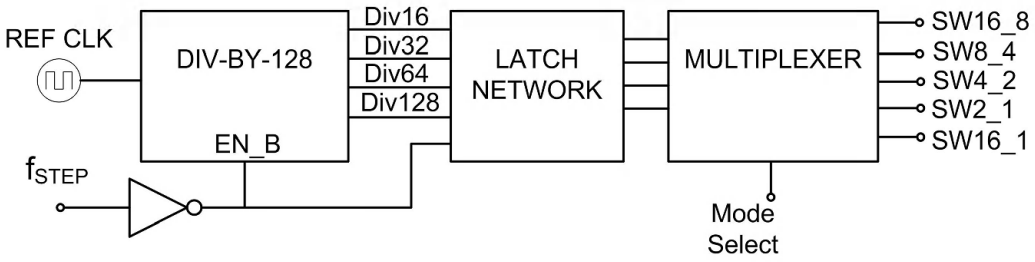

Figure 5-15 Implementation of Timing Control

5.7. Supplementary Blocks

The supplementary blocks perform such functions as resetting VCO control voltage on power up, probing out dc bias voltages for debug purposes and buffering VCO control voltage and N-Divider outputs to the pads.

5.7.1 V_{TUNE} Reset

The initial condition on V_{TUNE} after power up is very important, since if it rails, the synthesizer may never lock, due to charge pump, VCO or N-Divider failure. Figure 5-16 shows the circuit used to initialize V_{TUNE} on power up. It is essentially a voltage divider formed with MOS devices controlled by the reset signal (RST). When turned on, the PMOS and NMOS device resistances set V_{TUNE} to approximately the middle voltage of the charge pump supply. After reset is removed, the output is tri-stated for normal operation.

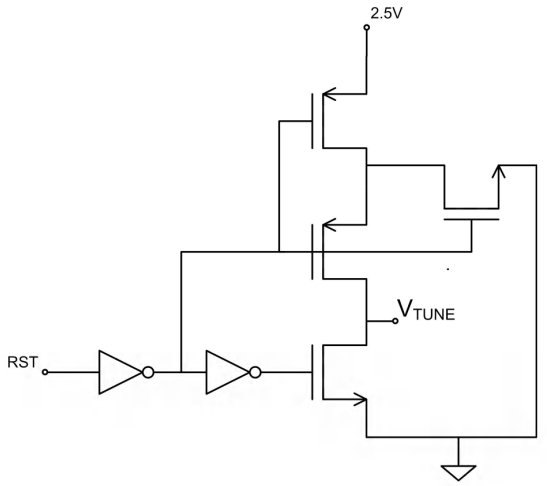

Figure 5-16 V_{TUNE} Initialization Circuit

5.7.2 DC Test (DCT)

Monitoring the bias voltages provides good insight into the debug process. Up to four bias voltages in various synthesizer blocks can be output to a single pin using DC switches forming a multiplexer. Two digital inputs select the bias voltage to be monitored as shown in Table 5-2. Figure 5-17 shows the DC test block.

Table 5-2 Selection of Internal Nodes for DC Test

Select Bits	Enable DCT of
00	Charge pump internal bias voltage
01	Loop filter internal node
10	Level-shifted VDD of SCL divide-by-2
11	Internal node of differential-to-single-ended converter

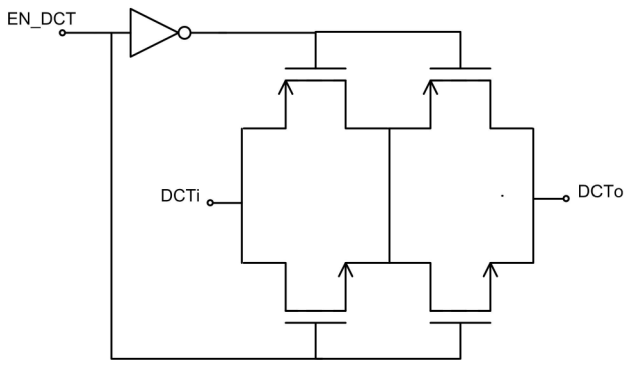

Figure 5-17 DC Test Block

The minimum sized switches allow only DC or very low frequency signals to pass through. Thus this test block is not useful for monitoring the VCO control voltage that has high frequency ripples. Instead a resized switch network is used as explained below.

5.7.3 V_{TUNE} Test

It is similar to the DC Test but the switches are designed such that the high frequency ripples on V_{TUNE} can be passed through the loading of the pad and package capacitances. The output pin driven by this block can be monitored during normal operation to observe the synthesizer locking behavior and measure the lock time. In the debug mode, the charge pump and the VCO performance can also be measured by connecting a fixed voltage source to this pin.

5.7.4 Output Buffer

The N-Divider output is buffered to the pad for monitoring on an oscilloscope and/or a spectrum analyzer. To drive the huge pad and package capacitance (~4.5pF), an inverter with $W_P = W_N = 30\mu m$ and $L_P=L_N=2L_{MIN}$ is used. Since this inverter operates on signals with very slow rise and fall times, a dedicated noisy supply is used for this inverter as shown in Figure 5-18. The noisy supply is dedicated implying it is not used anywhere in the core.

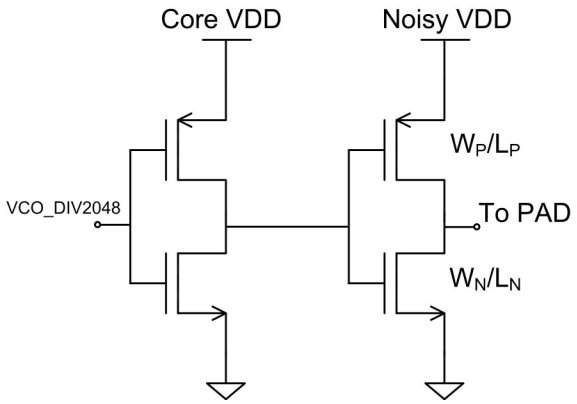

Figure 5-18 Output Buffer for Divided VCO Output

CHAPTER 6. SIMULATION RESULTS

6.1. Switching Time Simulation

6.1.1 Simulation Conditions

It is important to first consider simulation run times in a typical synthesizer simulation. As explained in [2], switching time simulation of a 2.4GHz synthesizer with a reference frequency of 1.172MHz requires few days of run time as well as significant CPU and memory resources. It thus becomes impractical to run iterative simulations. A "time contraction" technique that can speed up the simulation several times while preserving reasonable accuracy is also discussed in [2].

The same technique is used in this work for the switching time simulation with a contraction factor of 16. The reference frequency, division ratio and loop filter capacitors are scaled by this factor such that the loop bandwidth and the switching time are scaled correspondingly as shown in Table 6-1.

Table 6-1 Time Contraction Parameters

Parameter	Original	Scaled
f_R	1.172MHz	18.752MHz
N	2048	128
C_Z	727pF	45.4pF
C_P	138.5pF	8.65pF
f_C	10kHz	160kHz
t_{SW}	195μs	12.2μs

Since the reference period is now 53.33ns, the original PFD/CP combination with ~20ns dead-zone is not suitable for this simulation. Instead a modified version of original PFD/CP is used which has a dead-zone of ~2ns. Since the focus of this work is a 'comparison' of switching times in different adaptive and non-adaptive modes, scaled simulation results are expected to sufficiently serve as the benchmark for the anticipated experimental results.

6.1.2 One-Step and Four-Step Modes

Figure 6-1 shows the VCO control voltage transient for an output frequency step of 20.48MHz in one-step and four-step adaptive modes of the synthesizer. Two cases of one-step mode are presented – Case 1: One step occurs at the instant corresponding to the first step in the four-step mode, Case 2: One step occurs at the instant corresponding to the last step in the four-step mode. Case 2 is studied through simulation only whereas Case 1 can be studied though simulation as well as experimentally.

Table 6-2 shows the switching times (after multiplying by the scaling factor) for 0.1% error tolerance for four-step mode and Case 2 of one-step mode (best case). A 14% improvement is achieved in the four-step mode.

Table 6-2 Summary of Switching Times (Transistor-Level Simulation)

20.48MHz step 0.1% error	
Four-steps	**One-step (Case 2)**
96.4μs	112.6μs

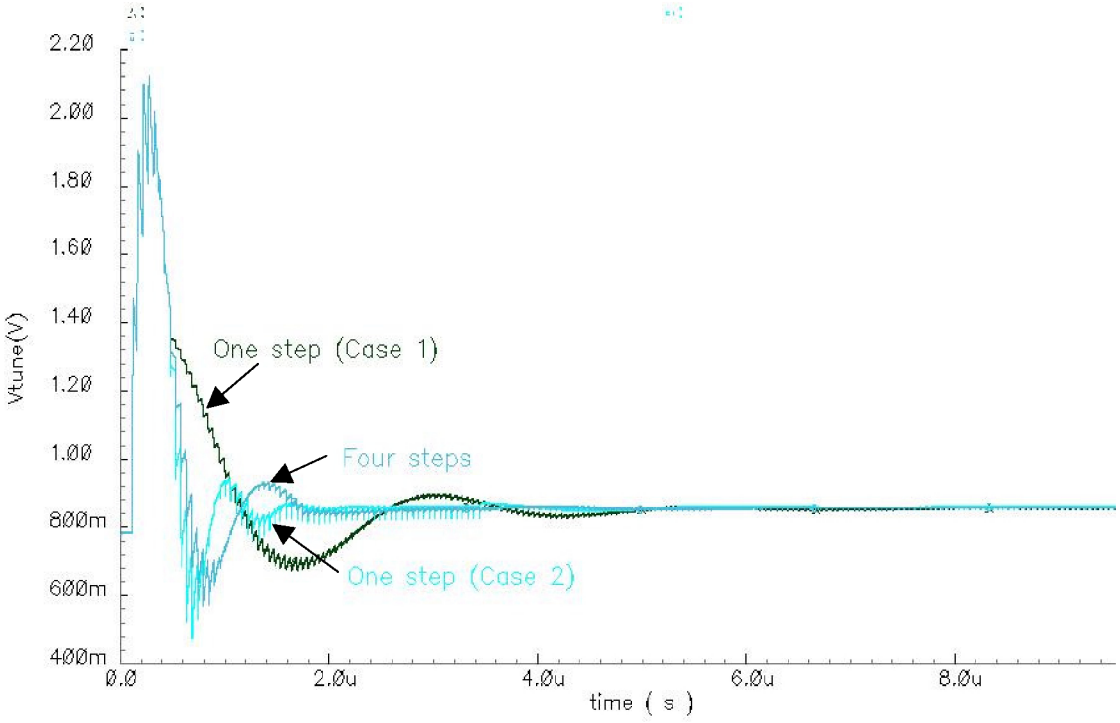

Figure 6-1 Switching Time Simulation (Transistor-Level): One-step and Four-step modes

6.2. VCO Simulation

The main performance parameters of the VCO are its tuning range and phase noise. Figure 6-2 and Figure 6-3 show respectively the tuning characteristics and the phase noise of the 2.41GHz VCO output. Table 6-3 summarizes the simulated VCO performance.

Table 6-3 VCO Simulation Results

Tuning Range (Coarse setting "0000")	7.4%
K_{VCO} @2.41GHz	258MHz/V
Phase Noise @3MHz	-127dBc/Hz
Power Consumption	3mA@2.5V

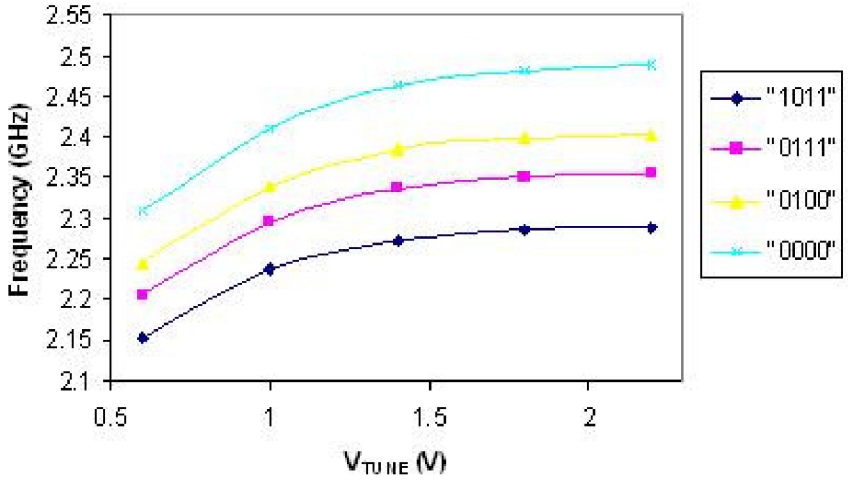

Figure 6-2 VCO Simulated Tuning Curves

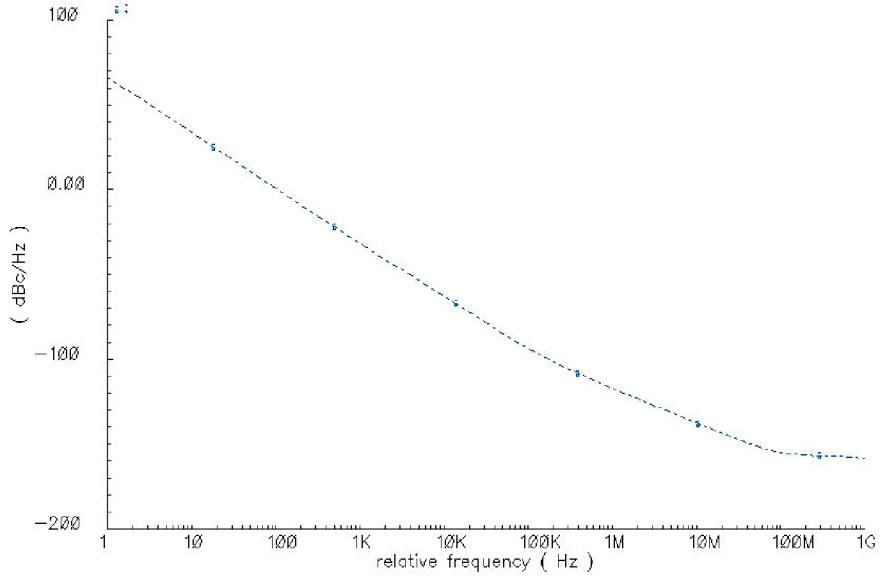

Figure 6-3 VCO Phase Noise

6.3. Charge Pump Simulation

The functionality of the PFD and charge pump is verified by using the PFD inputs REF and OSC that lead/lag with respect to each other. Figure 6-4 shows the simulation of OSC input lagging the REF input by 90°. The resulting UP current causes V_{LPF} to ramp up. Similarly a lead in the OSC input with respect to the REF input causes V_{LPF} to ramp-down.

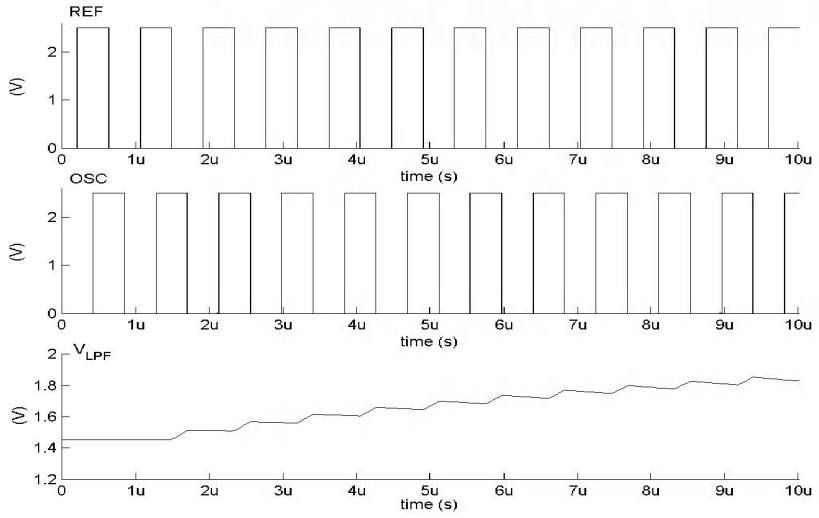

Figure 6-4 Charge Pump Output when OSC lags REF by 90°

Apart from the functional simulation, the V_{LPF} range and turn-on/off times of the charge pump are simulated. These parameters affect the VCO and the PFD designs. The results are summarized in Table 6-4.

6.4. SCL Divider Simulation

The maximum input frequency and power consumption are the main performance parameters for SCL dividers. The SCL Div-by-8 has a maximum operating frequency > 3GHz and consumes 625μA at 2.5V supply. Figure 6-5 shows the divider input from the VCO at 2.4GHz and the divider output.

Table 6-4 Charge Pump Simulation Results

Parameter	Simulated value	Comments
V_{LPF}	0.6 – 2.2 V	Worst case
t_{ON}/t_{OFF}	15.6ns/15.4ns	Dead-zone > 20ns
Power Consumption	776μA@3.3V	In Locked state

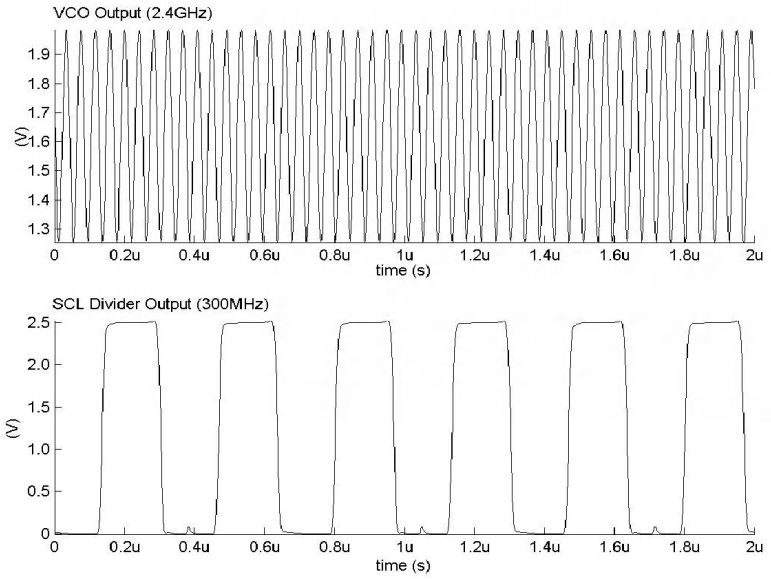

Figure 6-5 SCL Div-by-8 Output for VCO Output at 2.4GHz

CHAPTER 7. EXPERIMENTAL RESULTS

7.1. Layout and Fabrication

The frequency synthesizer is fabricated in the TSMC 0.25µm 2.5V mixed-mode process with 5 Metal layers and 1 Poly layer. The mixed-mode version of the process offers the following options suitable for mixed-signal designs such as the synthesizer:

- Thick-top Metal
- MiM Capacitors
- Thick-oxide devices
- Non-Epitaxial Wafers

All the building blocks described in Chapter 5 are integrated on-chip. The total die area is 2.62 x 2.62 mm^2 including bonding pads. Figure 7-1 shows the chip micrograph of the synthesizer. The loop filter occupies nearly half of the core area (excluding bonding pads) of the chip mainly due to the capacitors. 28 bonding pads are used of which eight pads are used for the four power supplies shown in Table 7-1.

Table 7-1 Chip Power Supplies

Power Supply	Nominal Voltage	Parts of Chip Supplied
VDD_DIG	2.5V	PFD, Digital divider, Timing control, Reference multiplexer, DC Test
VDD_VCO	2.5V	VCO, SCL divider, V_{TUNE} Reset
VDD_CP	3.3V	Charge pump, V_{TUNE} Buffer
VDD_BUF	2.5V	Divider output buffer

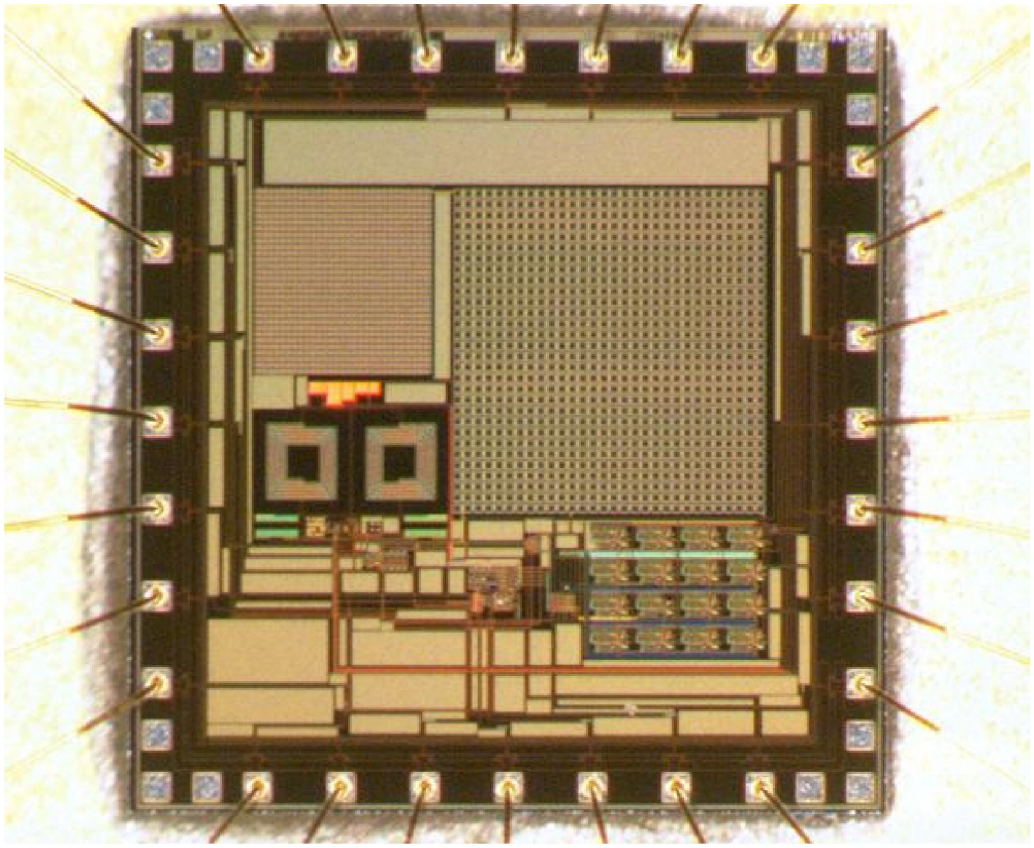

Figure 7-1 Synthesizer Chip Micrograph

Conventional layout practices such as common-centroid and inter-digitization are used wherever symmetry and matching are important such as in the differential VCO, Charge Pump current mirrors, Charge Pump array and the differential SCL dividers. IR drops in metal interconnects are also considered where critical e.g. the VCO and the LPF ground connection.

7.2. Pads and Packaging

The synthesizer is designed to fit in a 28-pin Ceramic Leadless Chip Carrier (LCC) package. Conventional grounded-gate MOS (ggMOS) devices are used in the bond pads for ESD protection. Three different types of bond pads are used which differ in the configuration

of the ESD devices. These are the VDD pads, GND pads and Input/Output (I/O) pads shown in Figure 7-1.

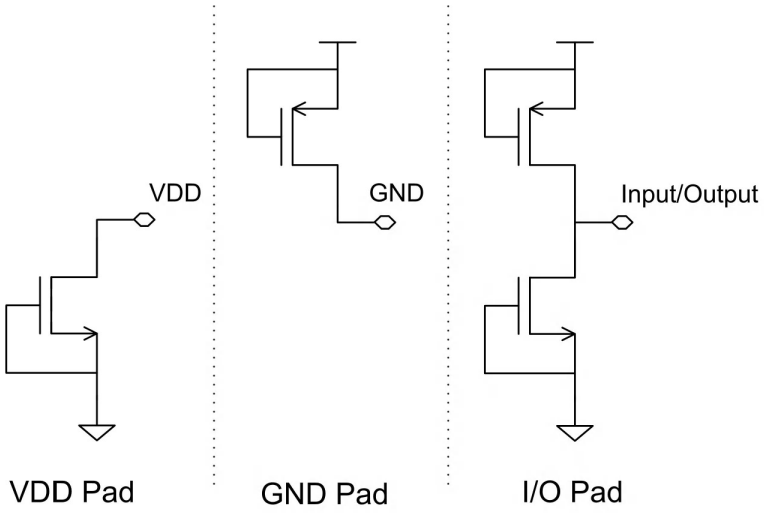

Figure 7-2 ESD Configuration

7.3. Test Results

A prototype board is built to measure the performance of the synthesizer in the laboratory. A simple 2-layer board is used without dedicated power or ground planes.

The primary measurement objective is the switching time in non-adaptive, one-step and four-step modes. The frequency step to be used for the measurement is set using two reference clock inputs of slightly different frequencies as already described. To measure the switching time, the VCO control voltage can be monitored and/or the frequencies of the two PFD inputs can be compared with respect to time.

The laboratory measurement set up is shown in Figure 7-3. Figure 7-4 shows the measured VCO control voltage and the PFD input waveforms on power-up. It was observed that the VCO control voltage was quickly railing to the supplies with small adjustments in the reference frequency around the anticipated 'lock' frequency. A stable lock condition was never achieved preventing any further measurements of switching time. Root cause of lock

failure could not be evaluated due to time factor however asymmetry in PFD layout, control voltage overshoots resulting in VCO and/or N-Divider failure and the huge variation in K_{VCO} across the tuning range are some of the potential causes for failure. A second fabrication cycle would help resolve some of these issues.

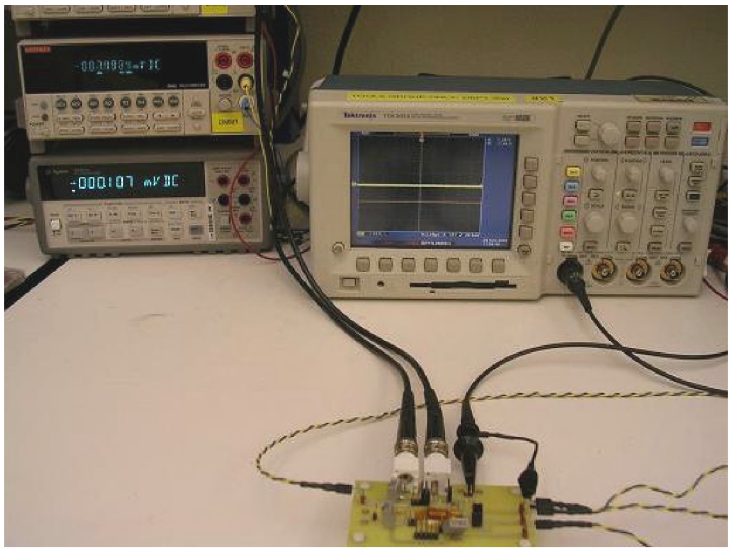

Figure 7-3 Measurement Setup

Figure 7-4 Measured V_{TUNE} (Averaged) and PFD Inputs (~1.2MHz) (1V/Div)

CHAPTER 8. CONCLUSIONS

In this thesis, an existing adaptive bandwidth solution to relax the design trade-off in fast-switching low-spurious frequency synthesizers is made more efficient by using a multi-step switching scheme for restoring the bandwidth from high to nominal thereby optimizing the total switching time. Behavioral simulations on Fractional-N and Integer-N adaptive bandwidth synthesizers using the proposed scheme provided satisfactory results for building a proof-of-concept test chip. A 2.4GHz Integer-N synthesizer is designed and fabricated in the TSMC 0.25μm mixed-signal CMOS process. Simulation of the whole synthesizer at the transistor-level showed a 14% improvement in switching time in four-step mode when compared to the best case of the one-step mode. The measurement of switching time could not be performed due to the intermittent locking behavior of the synthesizer on power-up. The behavioral and transistor-level simulations demonstrated the effectiveness of the proposed solution. A thoroughly optimized bandwidth switching sequence specific to the application would make the proposed solution a potential candidate for various fast frequency hopping systems.

BIBLIOGRAPHY

[1] Y. Tang, Y. Zhou, S. Bibykl, M. Ismail. A low noise fast settling PLL with extended loop bandwidth enhancement by new adaptation technique. *Proceedings of ASIC/SOC Conference, pp 93-97,* 2001.

[2] T.C. Lee, B. Razavi. A stabilization technique for phase locked loop synthesizers. *IEEE Journal of Solid-State Circuits, Vol .38, Issue 6, pp 888-894,* June 2003.

[3] C.S. Vaucher. Architectures for RF Frequency Synthesizers. *Kluwer Academic Publishers,* 2002

[4] W. Rhee. Design of high-performance CMOS charge pumps in phase-locked loops. *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, Vol. 2, pp 545-548,* 1999.

[5] J.R. Smith. Modern Communication Circuits. *WCB/Mc Graw Hill,* 1998.

[6] C.S. Vaucher. An adaptive PLL tuning system architecture combining high spectral purity and fast settling time. *IEEE Journal of Solid-State Circuits, Vol. 35, Issue 4, pp 490-502,* April 2000.

[7] M. Keaveney, P. Walsh, M. Tuthill, C. Lycen, B. Hunt. A 10μs fast switching PLL synthesizer for GSM/EDGE base-station. *ISSCC 2004 Digest of Technical Papers,* 2004.

[8] P. Kinget. Integrated GHz Voltage Controlled Oscillators. *Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators, pp 353-381, Kluwer Academic Publishers*, 1999

[9] D.M.W. Leenaerts, C.S. Vaucher, H.J. Bergveld, M. Thompson, K. Moore. A 15-mW fully integrated I/Q synthesizer for Bluetooth in 0.18-μm CMOS. *IEEE Journal of Solid-State Circuits, Vol .38, Issue 7,* July 2003.

[10] B. Zhang, P.E. Allen, J.M. Huard. A fast switching PLL frequency synthesizer with an on-chip passive discrete-time loop filter in 0.25-μm CMOS. *IEEE Journal of Solid-State Circuits, Vol .38, Issue 6, pp 855-865,* June 2003.

[11] J.R. Alexovich, R.M. Gagliardi. Effect of PLL frequency synthesizer in FSK frequency-hopped communications. *IEEE Transactions on Communications, Vol. 37, Issue 3, pp 268-276,* March 1989.

[12] C.W. Lo, H.C. Luong. A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications. *IEEE Journal of Solid-State Circuits, Vol .37, Issue 4, pp 459-470,* April 2002.

[13] J. Craninckx, M.S.J. Steyaert. A fully integrated CMOS DCS-1800 frequency synthesizer. *IEEE Journal of Solid-State Circuits, Vol .33, Issue 12, pp 2054-2065,* Dec 1998.

.

ACKNOWLEDGEMENTS

I would like to thank my advisor Professor Randall Geiger for his continued support and encouragement throughout my graduate studies and for letting me work on a thesis topic outside of his current research interests. I am also thankful to Professor Degang Chen for his guidance on control systems topics related to my thesis and for kindly agreeing to be part of my thesis committee.

The major part of my thesis was completed off-campus during which time many fellow students in my graduate program helped me on various issues, which otherwise required my presence on-campus. I am greatly indebted to all of them especially Vipul Katyal, Su Chao and Imad Abbadi. My sincere thanks to Yonghui Tang for allowing me to use his pad frame with my test chip.

I am grateful to the personnel of the MOSIS Educational Program for their consideration towards fabrication of my test chip in spite of some delays in layout submission. Special thanks are due to my colleagues at Marvell Semiconductor; Andalib Chowdhury for his experienced yet friendly advice on matters relating to design, fabrication and prototyping, Sasan Cyrusian for providing valuable debugging tips and Arnel Espejo for his diligence in assembling the prototype board.